



P67H2-A

Rev : 1.1

ECS
CONFIDENTIAL

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REVISION HISTORY:

Rev	Date	Notes
V.A	2010/05/04	Initial version
V.B	2010/06/15	Lucid HYDRA Core
V.1.0	2010/08/13	Integrated Clock Mode
V.1.1	2010/09/07	I-POD Charge Support

RD - ELI
LAYOUT : RITA

NOTE:
Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev1_01,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Revlp0.zip

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PCB Impedance control

Impedance (OHM)	Trace Width (mil)	(S/W/S)	Trace Length (inch)	Pre-preg	Default
50	4	(16/4/16)	8	1080	TOP BOTTOM
60	5	(20/5/20)	10	2116	INT

1)Circuit type 1

PCB STACK:

Layer 1:TOP

Layer 2:PWR

Layer 3:INT1

Layer 4:INT2

Layer 5:GND

Layer 6:BOTTOM

VCC3 IP

Trace on layer 1

Trace on layer 6

15-R97-011100 PCB M/B.P67H2-A.V1.1
..W/ECSLOGO..305*244*1.6mm.6L..LEADFREE..BLACK..OSP..GE1

ECS

Elitegroup Computer Systems

Title

COVER PAGE

Size

Custom

Document Number

P67H2-A

Rev

1.1

Date:

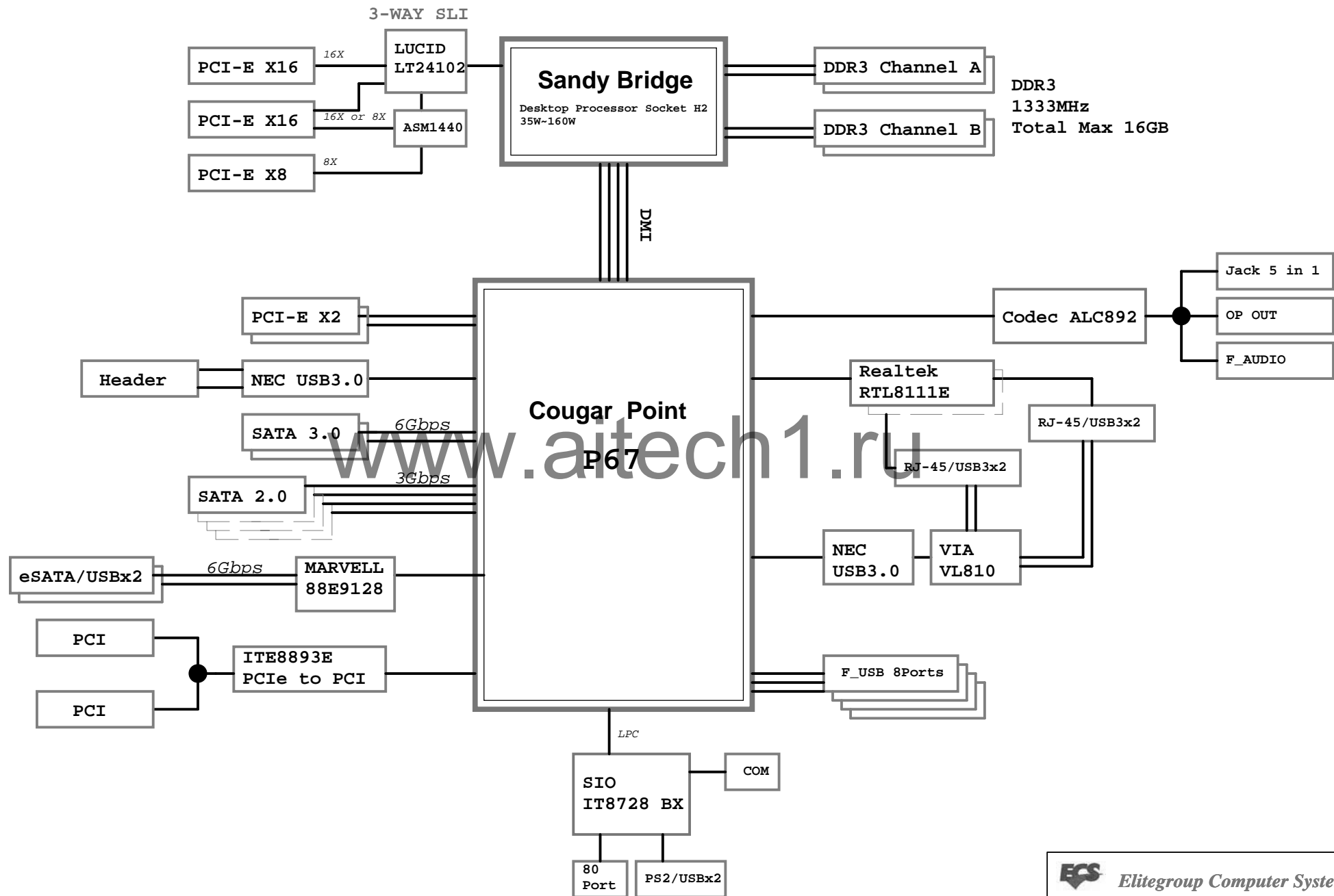
Wednesday, September 15, 2010

Sheet

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7 M_DATA_A[0..63]	← M_DATA A[0..63]
7 M_DQS_A_P[0..7]	← M_DQS A P[0..7]
7 M_DQS_A_N[0..7]	← M_DQS A N[0..7]
7 M_MA_A[0..15]	← M_MA A[0..15]
7 M_BS_A[0..2]	← M_BS A[0..2]
7 M_CS_A_L[0..3]	← M_CS A_L[0..3]
7 M_CKE_A[0..3]	← M_CKE A[0..3]
7 M_ODT_A[0..3]	← M_ODT A[0..3]
7 M_CLK_A_P[0..3]	← M_CLK A_P[0..3]
7 M_CLK_A_N[0..3]	← M_CLK A_N[0..3]
7 M_WE_A_L	← M_WE A_L
7 M_CAS_A_L	← M_CAS A_L
7 M_RAS_A_L	← M_RAS A_L

DDR3 CH.A

7,8 DDR3_DRAMRST_L ← DDR3_DRAMRST_L

8 M_DATA_B[0..63]	← M_DATA B[0..63]
8 M_DQS_B_P[0..7]	← M_DQS B P[0..7]
8 M_DQS_B_N[0..7]	← M_DQS B N[0..7]
8 M_MA_B[0..15]	← M_MA B[0..15]
8 M_BS_B[0..2]	← M_BS B[0..2]
8 M_CS_B_L[0..3]	← M_CS B_L[0..3]
8 M_CKE_B[0..3]	← M_CKE B[0..3]
8 M_ODT_B[0..3]	← M_ODT B[0..3]
8 M_CLK_B_P[0..3]	← M_CLK B_P[0..3]
8 M_CLK_B_N[0..3]	← M_CLK B_N[0..3]
8 M_WE_B_L	← M_WE B_L
8 M_CAS_B_L	← M_CAS B_L
8 M_RAS_B_L	← M_RAS B_L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0
M_DATA_A1	AJ4	SA_DQ_1
M_DATA_A2	AL3	SA_DQ_2
M_DATA_A3	AL4	SA_DQ_3
M_DATA_A4	AJ2	SA_DQ_4
M_DATA_A5	AJ1	SA_DQ_5
M_DATA_A6	AL2	SA_DQ_6
M_DATA_A7	AL1	SA_DQ_7
M_DATA_A8	AN1	SA_DQ_8
M_DATA_A9	AN4	SA_DQ_9
M_DATA_A10	AR3	SA_DQ_10
M_DATA_A11	AR4	SA_DQ_11
M_DATA_A12	AN2	SA_DQ_12
M_DATA_A13	AR2	SA_DQ_13
M_DATA_A14	AR2	SA_DQ_14
M_DATA_A15	AR1	SA_DQ_15
M_DATA_A16	AV2	SA_DQ_16
M_DATA_A17	AW3	SA_DQ_17
M_DATA_A18	AV5	SA_DQ_18
M_DATA_A19	AV5	SA_DQ_19
M_DATA_A20	AU2	SA_DQ_20
M_DATA_A21	AU3	SA_DQ_21
M_DATA_A22	AU5	SA_DQ_22
M_DATA_A23	AY5	SA_DQ_23
M_DATA_A24	AY7	SA_DQ_24
M_DATA_A25	AU7	SA_DQ_25
M_DATA_A26	AV9	SA_DQ_26
M_DATA_A27	AU9	SA_DQ_27
M_DATA_A28	AV7	SA_DQ_28
M_DATA_A29	AW7	SA_DQ_29
M_DATA_A30	AR1	SA_DQ_30
M_DATA_A31	AY9	SA_DQ_31
M_DATA_A32	AU35	SA_DQ_32
M_DATA_A33	AW37	SA_DQ_33
M_DATA_A34	AU39	SA_DQ_34
M_DATA_A35	AU36	SA_DQ_35
M_DATA_A36	AW35	SA_DQ_36
M_DATA_A37	AY36	SA_DQ_37
M_DATA_A38	AU38	SA_DQ_38
M_DATA_A39	AU37	SA_DQ_39
M_DATA_A40	AR40	SA_DQ_40
M_DATA_A41	AR37	SA_DQ_41
M_DATA_A42	AN35	SA_DQ_42
M_DATA_A43	AN37	SA_DQ_43
M_DATA_A44	AR39	SA_DQ_44
M_DATA_A45	AR38	SA_DQ_45
M_DATA_A46	AN39	SA_DQ_46
M_DATA_A47	AN40	SA_DQ_47
M_DATA_A48	AL40	SA_DQ_48
M_DATA_A49	AL37	SA_DQ_49
M_DATA_A50	AJ38	SA_DQ_50
M_DATA_A51	AJ37	SA_DQ_51
M_DATA_A52	AJ38	SA_DQ_52
M_DATA_A53	AJ38	SA_DQ_53
M_DATA_A54	AJ40	SA_DQ_54
M_DATA_A55	AG40	SA_DQ_55
M_DATA_A56	AG37	SA_DQ_56
M_DATA_A57	AE38	SA_DQ_57
M_DATA_A58	AE37	SA_DQ_58
M_DATA_A59	AG39	SA_DQ_59
M_DATA_A60	AG38	SA_DQ_60
M_DATA_A61	AE39	SA_DQ_61
M_DATA_A62	AE38	SA_DQ_62
M_DATA_A63	AE40	SA_DQ_63

M_DQS_A_P0	AK3	SA_DQS_0
M_DQS_A_P1	AP3	SA_DQS_1
M_DQS_A_P2	AW4	SA_DQS_2
M_DQS_A_P3	AV8	SA_DQS_3
M_DQS_A_P4	AV37	SA_DQS_4
M_DQS_A_P5	AP38	SA_DQS_5
M_DQS_A_P6	AK38	SA_DQS_6
M_DQS_A_P7	AF38	SA_DQS_7

M_DQS_A_N0	AK2	SA_DQS#_0
M_DQS_A_N1	AP2	SA_DQS#_1
M_DQS_A_N2	AV4	SA_DQS#_2
M_DQS_A_N3	AW8	SA_DQS#_3
M_DQS_A_N4	AV36	SA_DQS#_4
M_DQS_A_N5	AP39	SA_DQS#_5
M_DQS_A_N6	AK39	SA_DQS#_6
M_DQS_A_N7	AF39	SA_DQS#_7

BALLMAP_REV=1.4

SA_MA_0	AV27	M_MA_A0
SA_MA_1	AV24	M_MA_A1
SA_MA_2	AW24	M_MA_A2
SA_MA_3	AW23	M_MA_A3
SA_MA_4	AV23	M_MA_A4
SA_MA_5	AT24	M_MA_A5
SA_MA_6	AT23	M_MA_A6
SA_MA_7	AJ24	M_MA_A7
SA_MA_8	AV22	M_MA_A8
SA_MA_9	AT22	M_MA_A9
SA_MA_10	AV28	M_MA_A10
SA_MA_11	AJ21	M_MA_A11
SA_MA_12	AT21	M_MA_A12
SA_MA_13	AW32	M_MA_A13
SA_MA_14	AJ20	M_MA_A14
SA_MA_15	AT20	M_MA_A15

SA_WE#	AW29	M_WE_A_L
SA_CAS#	AV30	M_CAS_A_L
SA_RAS#	AJ28	M_RAS_A_L

SA_BS_0	AY29	M_BS_A0
SA_BS_1	AW28	M_BS_A1
SA_BS_2	AV20	M_BS_A2

SA_CS#_0	AJ29	M_CS_A_L0
SA_CS#_1	AV32	M_CS_A_L1
SA_CS#_2	AW30	M_CS_A_L2
SA_CS#_3	AJ33	M_CS_A_L3

SA_CKE_0	AV19	M_CKE_A0
SA_CKE_1	AT19	M_CKE_A1
SA_CKE_2	AJ18	M_CKE_A2
SA_CKE_3	AV18	M_CKE_A3

SA_ODT_0	AV31	M_ODT_A0
SA_ODT_1	AJ32	M_ODT_A1
SA_ODT_2	AJ30	M_ODT_A2
SA_ODT_3	AW33	M_ODT_A3

SA_CK_0	AY25	M_CLK_A_P0
SA_CK#_0	AW25	M_CLK_A_N0
SA_CK_1	AJ24	M_CLK_A_P1
SA_CK#_1	AW25	M_CLK_A_N1
SA_CK_2	AY27	M_CLK_A_P2
SA_CK#_2	AY27	M_CLK_A_N2
SA_CK_3	AY26	M_CLK_A_P3
SA_CK#_3	AW26	M_CLK_A_N3

SA_ECC_CB_0	AW18	DDR3_DRAMRST_R_L
SA_ECC_CB_1	AV13	
SA_ECC_CB_2	AV12	
SA_ECC_CB_3		
SA_ECC_CB_4		
SA_ECC_CB_5		
SA_ECC_CB_6		
SA_ECC_CB_7		

DDR_0

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SKT_H2_CRB

DDR3 CH.A

Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0
M_DATA_B1	AG8	SB_DQ_1
M_DATA_B2	AJ9	SB_DQ_2
M_DATA_B3	AJ8	SB_DQ_3
M_DATA_B4	AG5	SB_DQ_4
M_DATA_B5	AG6	SB_DQ_5
M_DATA_B6	AJ6	SB_DQ_6
M_DATA_B7	AJ7	SB_DQ_7
M_DATA_B8	AV7	SB_DQ_8
M_DATA_B9	AM7	SB_DQ_9
M_DATA_B10	AM10	SB_DQ_10
M_DATA_B11	AL10	SB_DQ_11
M_DATA_B12	AL6	SB_DQ_12
M_DATA_B13	AL6	SB_DQ_13
M_DATA_B14	AL9	SB_DQ_14
M_DATA_B15	AM9	SB_DQ_15
M_DATA_B16	AP7	SB_DQ_16
M_DATA_B17	AR7	SB_DQ_17
M_DATA_B18	AP10	SB_DQ_18
M_DATA_B19	AR10	SB_DQ_19
M_DATA_B20	AP6	SB_DQ_20
M_DATA_B21	AR6	SB_DQ_21
M_DATA_B22	AP9	SB_DQ_22
M_DATA_B23	AR9	SB_DQ_23
M_DATA_B24	AM12	SB_DQ_24
M_DATA_B25	AM13	SB_DQ_25
M_DATA_B26	AR13	SB_DQ_26
M_DATA_B27	AP13	SB_DQ_27
M_DATA_B28	AL12	SB_DQ_28
M_DATA_B29	AL13	SB_DQ_29
M_DATA_B30	AR12	SB_DQ_30
M_DATA_B31	AP12	SB_DQ_31
M_DATA_B32	AR28	SB_DQ_32
M_DATA_B33	AR29	SB_DQ_33
M_DATA_B34	AL28	SB_DQ_34
M_DATA_B35	AL29	SB_DQ_35
M_DATA_B36	AP28	SB_DQ_36
M_DATA_B37	AP29	SB_DQ_37
M_DATA_B38	AM28	SB_DQ_38
M_DATA_B39	AM29	SB_DQ_39
M_DATA_B40	AP32	SB_DQ_40
M_DATA_B41	AP31	SB_DQ_41
M_DATA_B42	AP35	SB_DQ_42
M_DATA_B43	AP34	SB_DQ_43
M_DATA_B44	AR32	SB_DQ_44
M_DATA_B45	AR31	SB_DQ_45
M_DATA_B46	AR35	SB_DQ_46
M_DATA_B47	AR34	SB_DQ_47
M_DATA_B48	AM32	SB_DQ_48
M_DATA_B49	AM31	SB_DQ_49
M_DATA_B50	AL35	SB_DQ_50
M_DATA_B51	AL32	SB_DQ_51
M_DATA_B52	AL31	SB_DQ_52
M_DATA_B53	AM35	SB_DQ_53
M_DATA_B54	AL34	SB_DQ_54
M_DATA_B55	AH35	SB_DQ_55
M_DATA_B56	AH34	SB_DQ_56
M_DATA_B57	AE34	SB_DQ_57
M_DATA_B58	AE35	SB_DQ_58
M_DATA_B59	AJ35	SB_DQ_59
M_DATA_B60	AJ35	SB_DQ_60
M_DATA_B61	AJ34	SB_DQ_61
M_DATA_B62	AF33	SB_DQ_62
M_DATA_B63	AF35	SB_DQ_63

M_DQS_B_P0	AH7	SB_DQS_0
M_DQS_B_P1	AM8	SB_DQS_1
M_DQS_B_P2	AR8	SB_DQS_2
M_DQS_B_P3	AN13	SB_DQS_3
M_DQS_B_P4	AN29	SB_DQS_4
M_DQS_B_P5	AP33	SB_DQS_5
M_DQS_B_P6	AL33	SB_DQS_6
M_DQS_B_P7	AG35	SB_DQS_7

M_DQS_B_N0	AH6	SB_DQS#_0
M_DQS_B_N1	AL8	SB_DQS#_1
M_DQS_B_N2	AP8	SB_DQS#_2
M_DQS_B_N3	AN12	SB_DQS#_3
M_DQS_B_N4	AN28	SB_DQS#_4
M_DQS_B_N5	AR32	SB_DQS#_5
M_DQS_B_N6	AM33	SB_DQS#_6
M_DQS_B_N7	AG34	SB_DQS#_7

CPU1D

BALLMAP_REV=1.4

SB_MA_0	AK24	M_MA_B0
SB_MA_1	AM20	M_MA_B1
SB_MA_2	AM19	M_MA_B2
SB_MA_3	AK18	M_MA_B3
SB_MA_4	AP19	M_MA_B4
SB_MA_5	AP18	M_MA_B5
SB_MA_6	AM18	M_MA_B6
SB_MA_7	AL18	M_MA_B7
SB_MA_8	AN18	M_MA_B8
SB_MA_9	AY17	M_MA_B9
SB_MA_10	AN23	M_MA_B10
SB_MA_11	AN17	M_MA_B11
SB_MA_12	AT18	M_MA_B12
SB_MA_13	AR26	M_MA_B13
SB_MA_14	AY16	M_MA_B14
SB_MA_15	AV16	M_MA_B15

SA_CK[2]	AR25	M_WE_B_L
SA_CK[1]	AK25	M_CAS_B_L
SA_ODT[2]	AP24	M_RAS_B_L

SB_BS_0	AP23	M_BS_B0
SB_BS_1	AM24	M_BS_B1
SB_BS_2	AW17	M_BS_B2

SB_CS#_0	AN25	M_CS_B_L0
SB_CS#_1	AN26	M_CS_B_L1
SB_CS#_2	AT25	M_CS_B_L2
SB_CS#_3	AT26	M_CS_B_L3

SB_CKE_0	AU16	M_CKE_B0
SB_CKE_1	AY15	M_CKE_B1
SB_CKE_2	AW15	M_CKE_B2
SB_CKE_3	AV15	M_CKE_B3

SB_ODT_0	AL26	M_ODT_B0
SB_ODT_1	AP26	M_ODT_B1
SB_ODT_2	AM26	M_ODT_B2
SB_ODT_3	AK26	M_ODT_B3

SB_CK_0	AL21	M_CLK_B_P0
SB_CK#_0	AL22	M_CLK_B_N0
SB_CK_1	AL20	M_CLK_B_P1
SB_CK#_1	AK20	M_CLK_B_N1
SB_CK_2	AL23	M_CLK_B_P2
SB_CK#_2	AM22	M_CLK_B_N2
SB_CK_3	AP21	M_CLK_B_P3
SB_CK#_3	AN21	M_CLK_B_N3

SB_ECC_CB_0	AN16	
SB_ECC_CB_1	AM16	
SB_ECC_CB_2	AP16	
SB_ECC_CB_3	AR16	
SB_ECC_CB_4	AL15	
SB_ECC_CB_5	AM15	
SB_ECC_CB_6	AR15	
SB_ECC_CB_7	AP15	

DDR_1

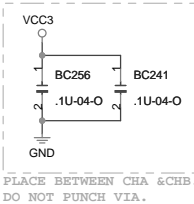
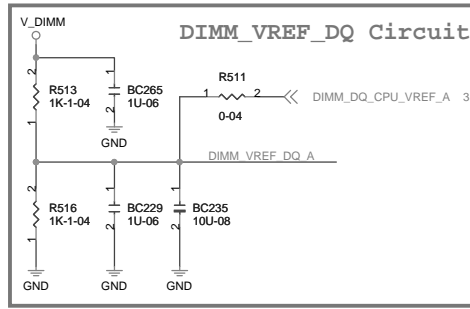
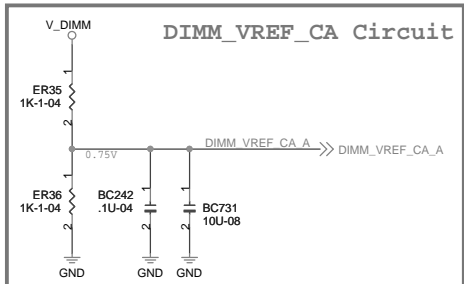
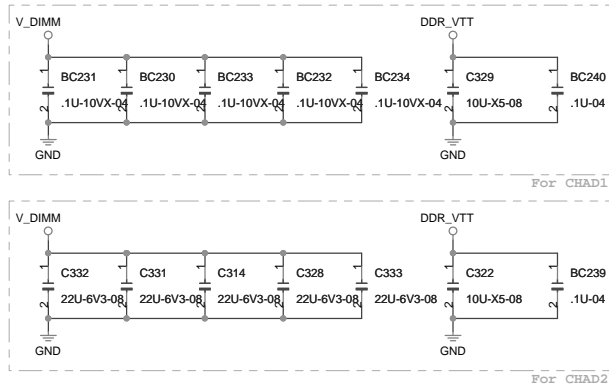
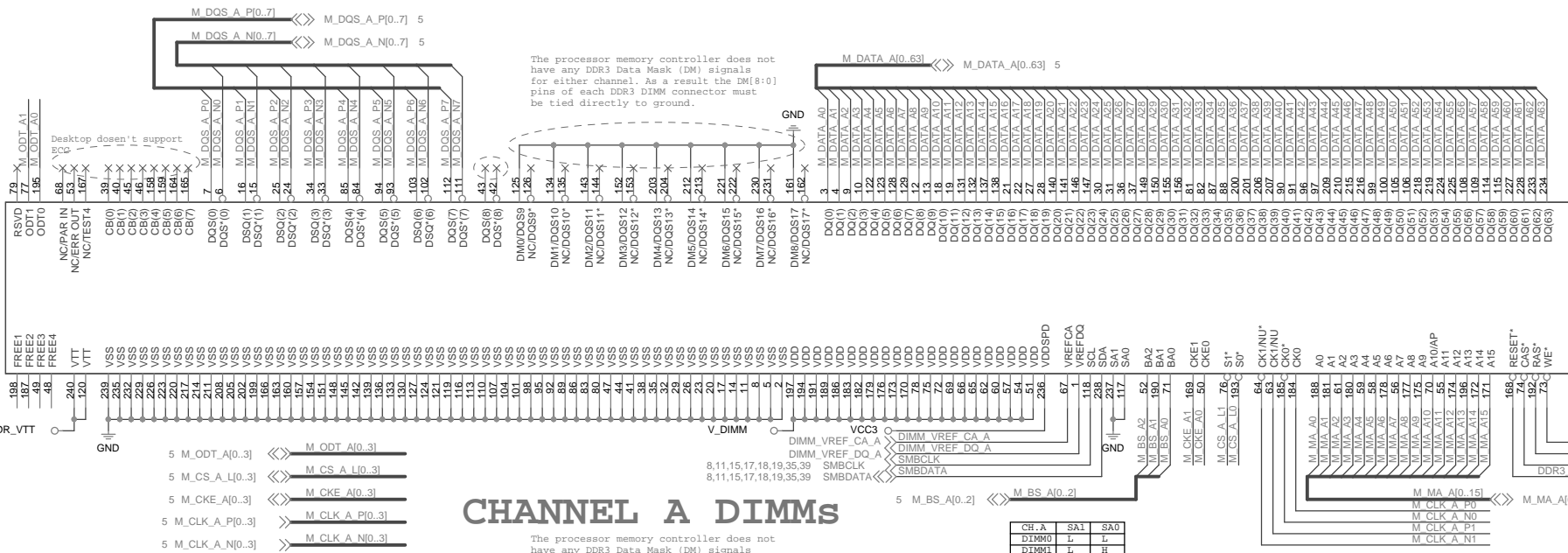
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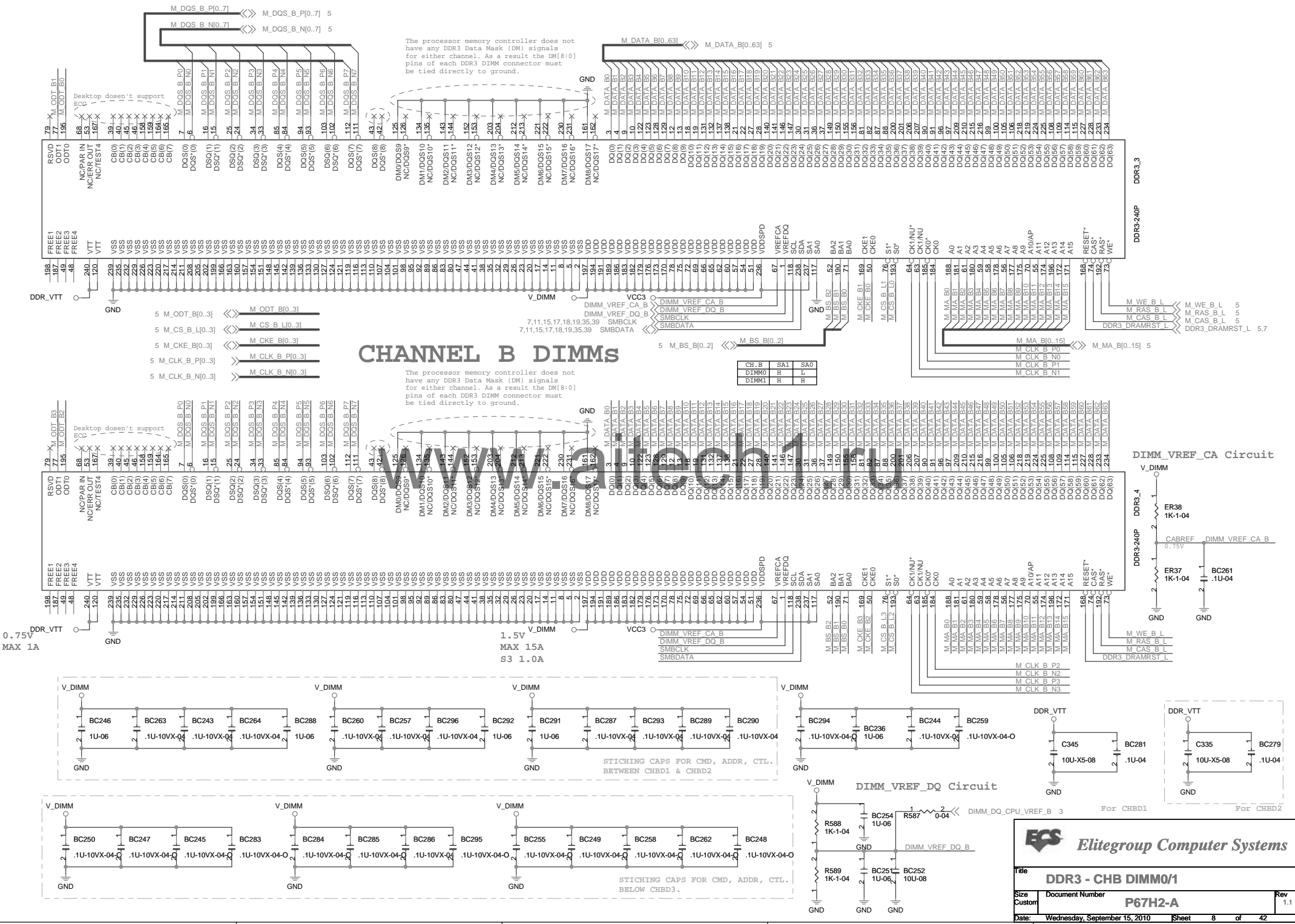
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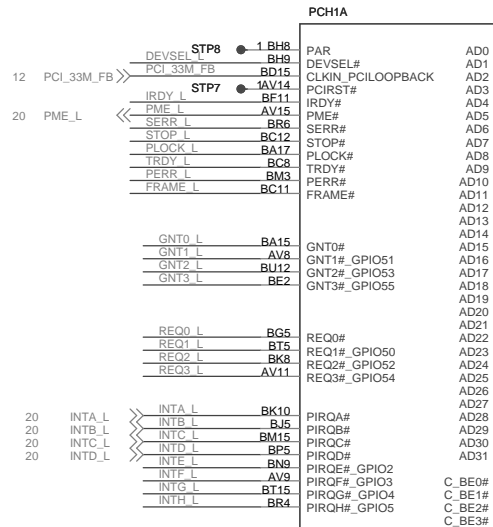
DDR3 CH.B



Title			CPU - DDR3
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Custom			Rev 1.1
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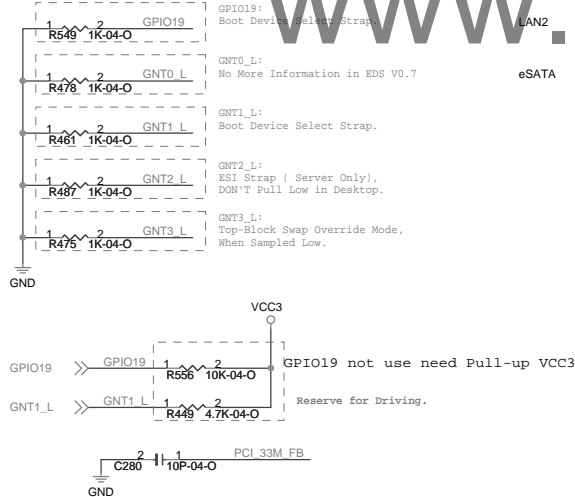


U1CPT

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GNT[0..3]#
GPIO19
have been internal pull high to +VCC3



PCI

USB3.0

USB3.0

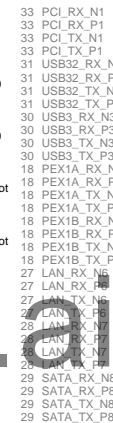
PCIe slot

PCIe slot

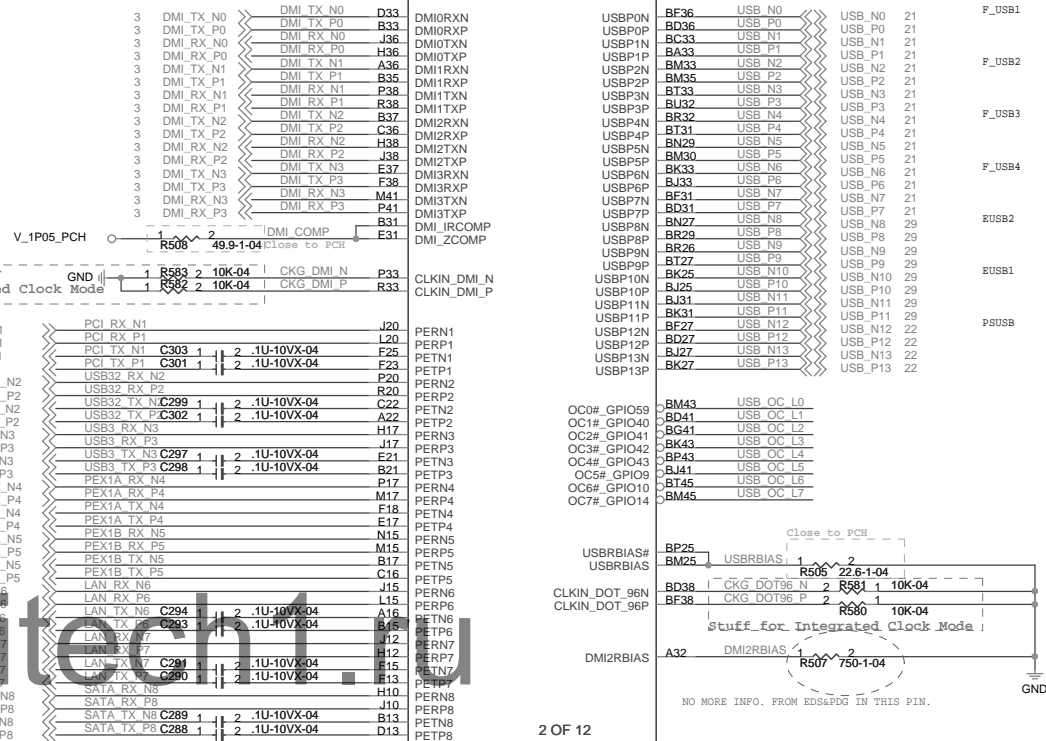
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LAN2

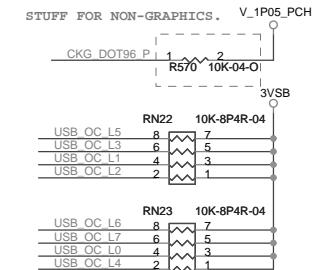
eSATA



PCH1B

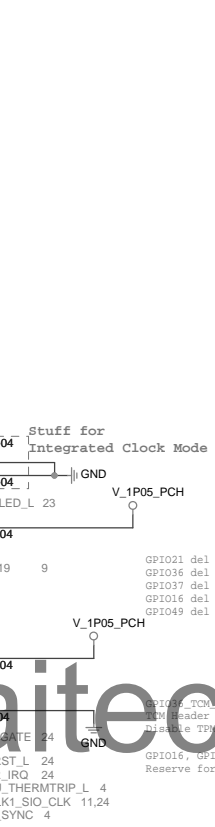
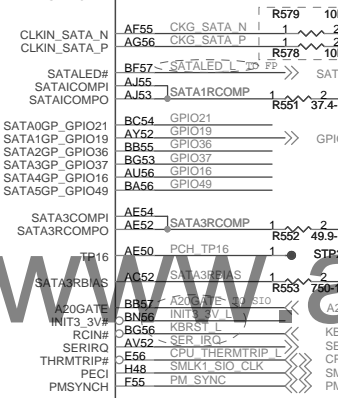
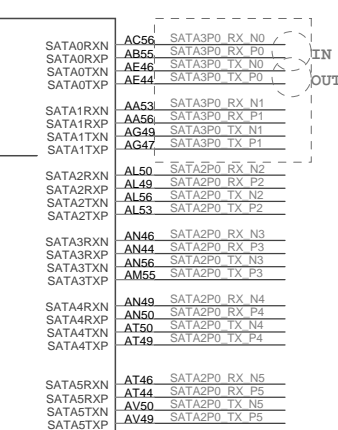
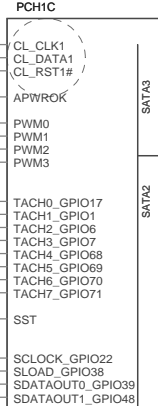
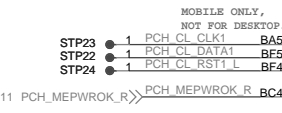


U1CPT



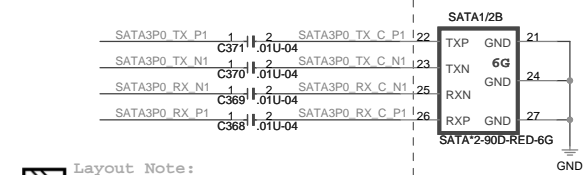
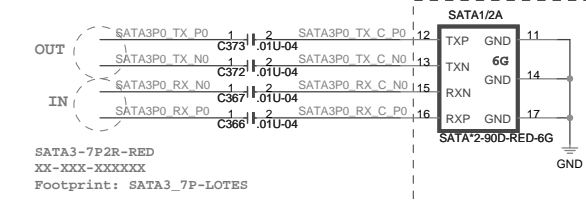
Elitegroup Computer Systems

Title			
PCH - DMI, PCI, PE, USB			
Size	Document Number	Rev	
Custom	P67H2-A	1.1	
Date:	Wednesday, September 15, 2010	Sheet	9 of 42

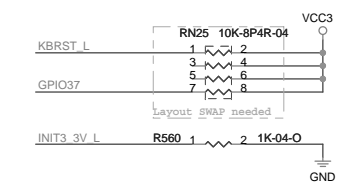
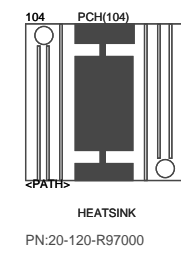
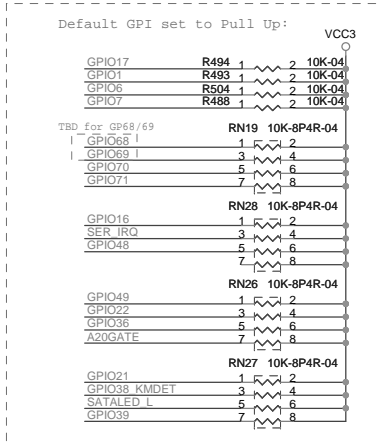
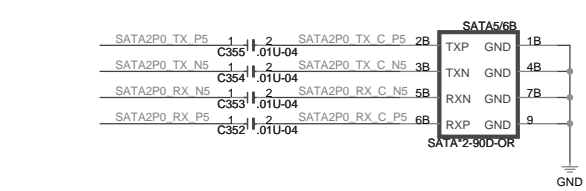
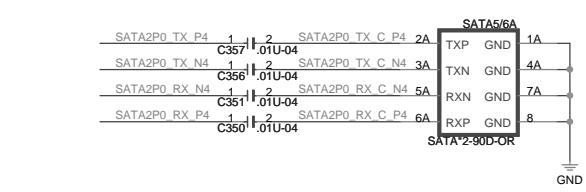
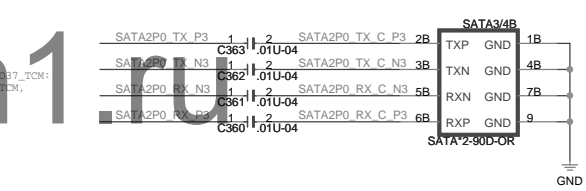
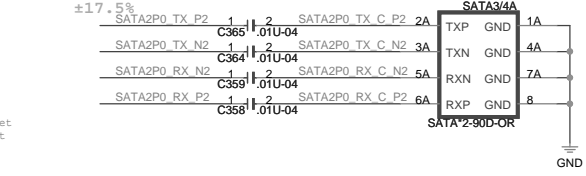


ONLY SATA PORT0 & PORT1 SUPPORT SATA 6Gbps

10-020-007069



Layout Note:
SATA3.0 4.5/7.5/20 in 90 Ω
±17.5%
SATA2.0 4.5/7.5/15 in 90 Ω
±17.5%

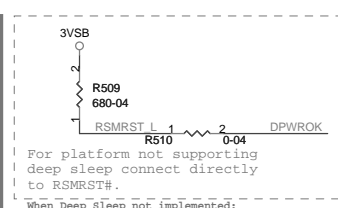
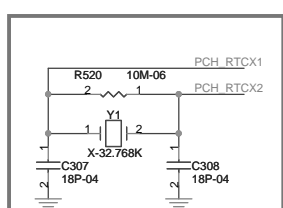
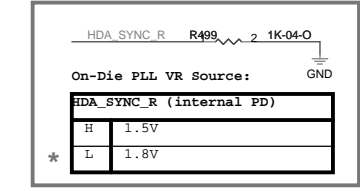
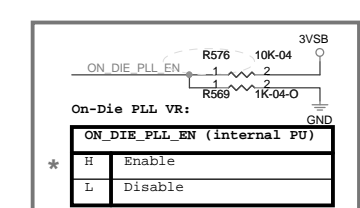
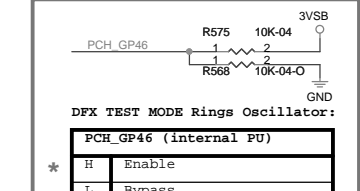
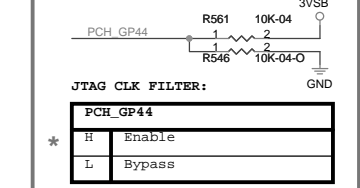
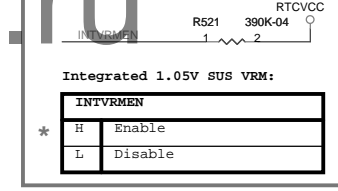
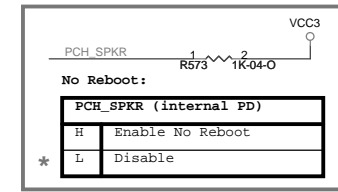
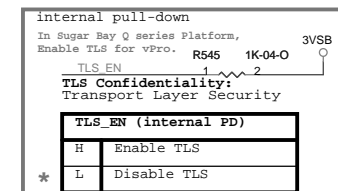
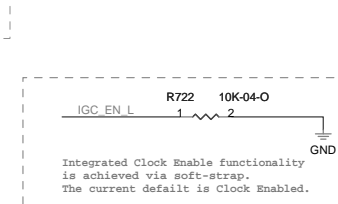
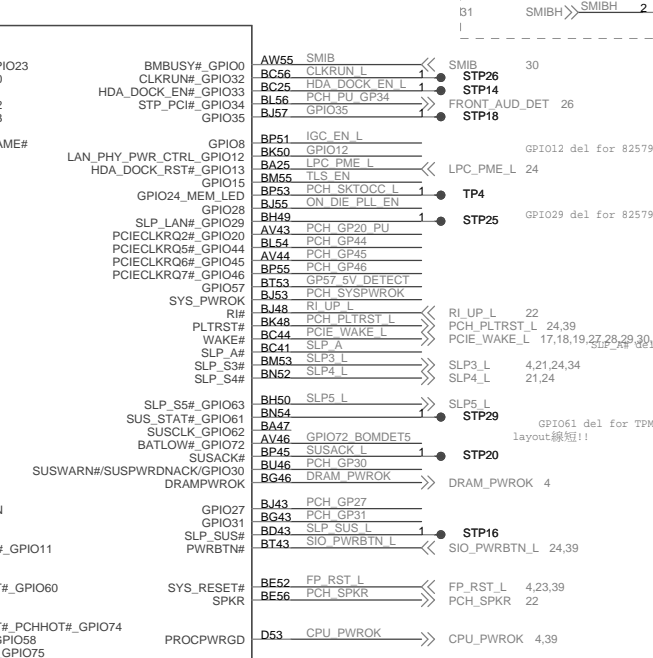
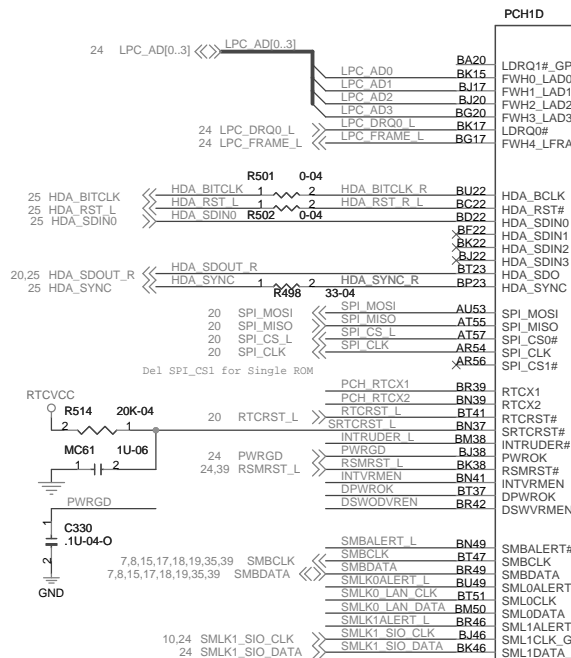


Elitegroup Computer Systems

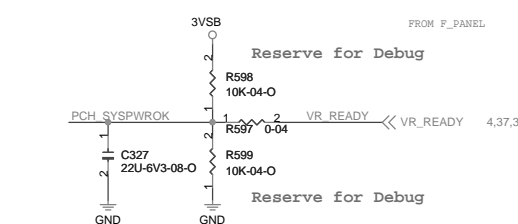
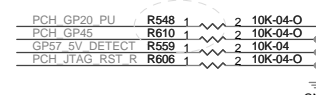
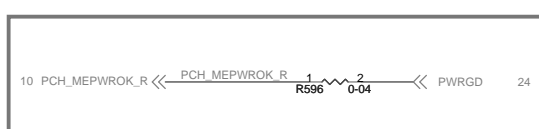
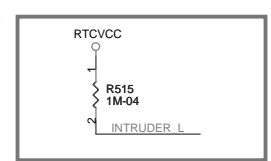
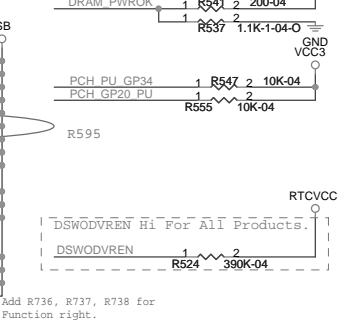
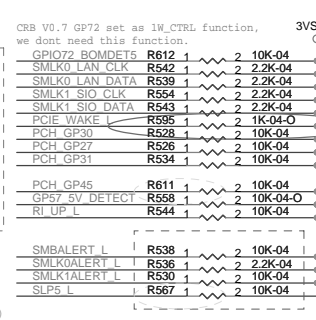
PCH - SATA, HEATSINK

Document Number P67H2-A

Date: Wednesday, September 15, 2010 Sheet 10 of 42

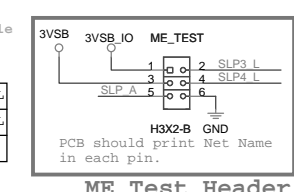


1. PCH_GP30, PCH_GP27 need to be Pull Up.
2. VCCSDW3.3 should be connected to +3VSB.
3. SLP_SUS_L, SUSACK_L left unconnected.
4. SUSWARN_L may be used as GPIO30. (Reference to 1.)



Layout Note: Print this table near ME_TEST

3VAX	S3_L
3VSB	S4_L
SA_L	GND



ME Test Header

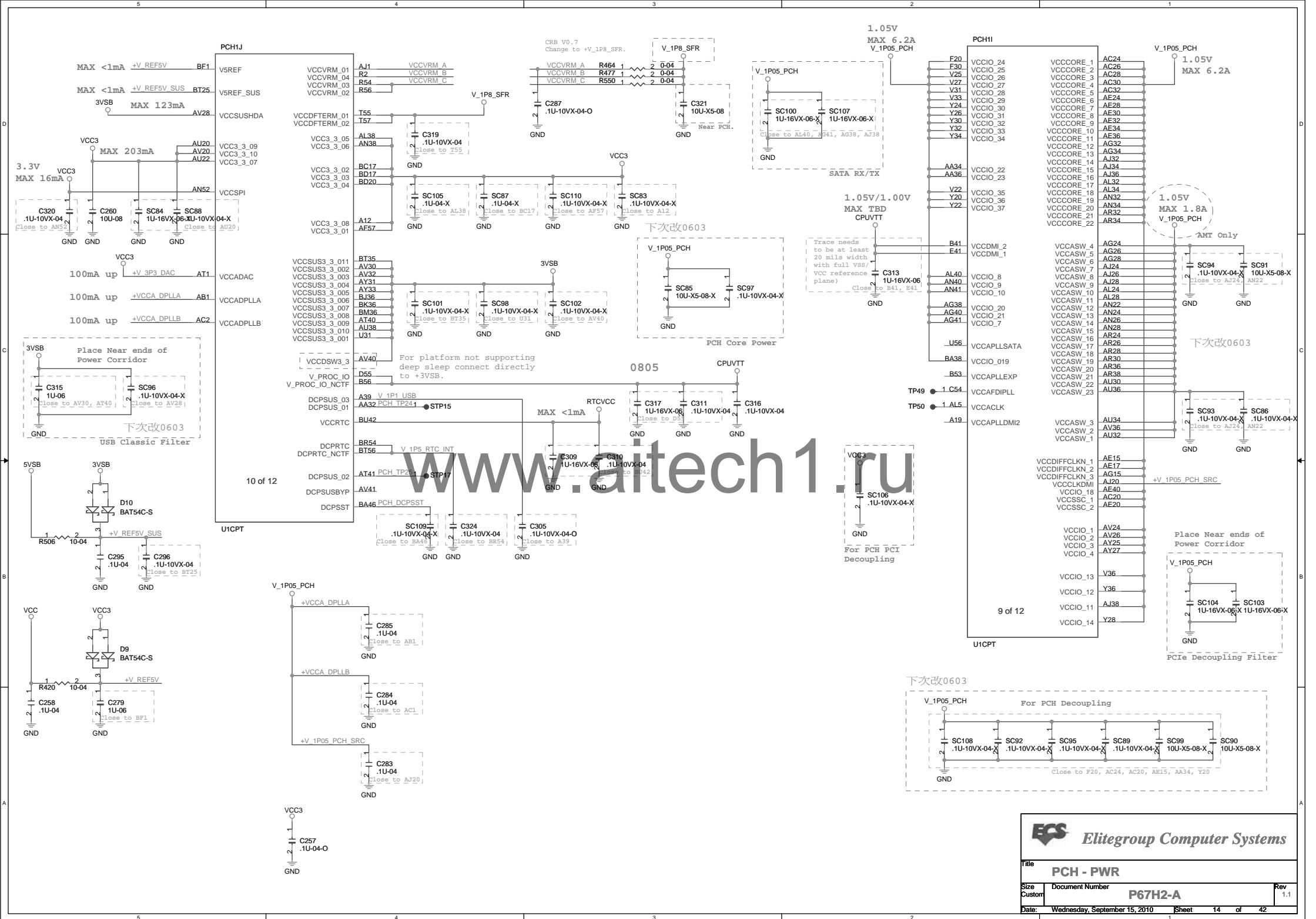
CASE Open Circuit

ECS Elitegroup Computer Systems

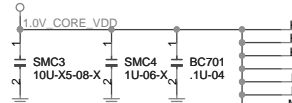
Title: **PCH - MISC, Strap Function**

Size: **Document Number** **P67H2-A** **Rev 1.1**

Date: **Wednesday, September 15, 2010** Sheet **11** of **42**



1.0VL

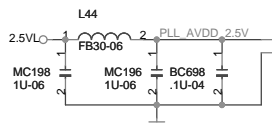


HDAF

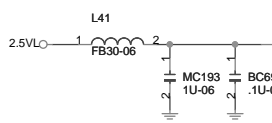
CORE_VDD[1]
CORE_VDD[2]
CORE_VDD[3]
CORE_VDD[4]
CORE_VDD[5]
CORE_VDD[6]
CORE_VDD[7]
CORE_VDD[8]
CORE_VDD[9]
CORE_VDD[10]
CORE_VDD[11]
CORE_VDD[12]

PEX_AVDD[1]
PEX_AVDD[2]
PEX_AVDD[3]
PEX_AVDD[4]
PEX_AVDD[5]
PEX_AVDD[6]
PEX_AVDD[7]
PEX_AVDD[8]
PEX_AVDD[9]
PEX_AVDD[10]
PEX_AVDD[11]
PEX_AVDD[12]
PEX_AVDD[13]
PEX_AVDD[14]
PEX_AVDD[15]
PEX_AVDD[16]
PEX_AVDD[17]
PEX_AVDD[18]

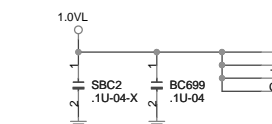
G7 2.5V PEX AVDD
G16
H7
H9
H14
H16
J14
P11
P12
R7
R9
R14
R16
T7
T9
T14
T16



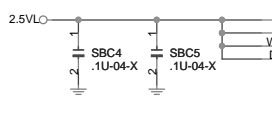
PLL_AVDD
PLL_AVSS



REFCLK_VDDIO

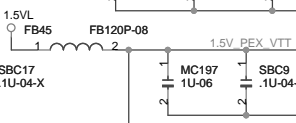
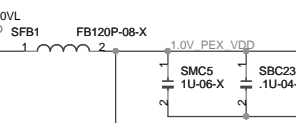
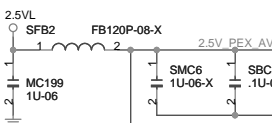
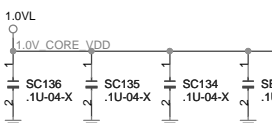


REFCLK_VDD[1]
REFCLK_VDD[2]
REFCLK_VDD[3]
REFCLK_VDD[4]



VDD_IO[1]
VDD_IO[2]
VDD_IO[3]
VDD_IO[4]

LT24102



PEX_VTT[1]
PEX_VTT[2]
PEX_VTT[3]
PEX_VTT[4]
PEX_VTT[5]
PEX_VTT[6]
PEX_VTT[7]
PEX_VTT[8]
PEX_VTT[9]
PEX_VTT[10]
PEX_VTT[11]
PEX_VTT[12]
PEX_VTT[13]
PEX_VTT[14]
PEX_VTT[15]
PEX_VTT[16]
PEX_VTT[17]
PEX_VTT[18]
PEX_VTT[19]
PEX_VTT[20]
PEX_VTT[21]
PEX_VTT[22]
PEX_VTT[23]
PEX_VTT[24]
PEX_VTT[25]
PEX_VTT[26]
PEX_VTT[27]

G6
G10
G13
G17
H6
H10
H13
H17
J13
K8
L6
L15
L17
M6
M8
M15
M17
P10
R6
R10
R13
R17
T6
T10
T13
T17

PEG16X RX P0 C588 1 2 .1U-10VX-04BR04 PE TXP0 A19
PEG16X RX N0 C587 1 2 .1U-10VX-04BR04 PE TXN0 B19
PEG16X RX P1 C585 1 2 .1U-10VX-04BR04 PE TXP1 A18
PEG16X RX N1 C586 1 2 .1U-10VX-04BR04 PE TXN1 B18
PEG16X RX P2 C590 1 2 .1U-10VX-04BR04 PE TXP2 B17
PEG16X RX N2 C589 1 2 .1U-10VX-04BR04 PE TXN2 C17
PEG16X RX P3 C583 1 2 .1U-10VX-04BR04 PE TXP3 A16
PEG16X RX N3 C584 1 2 .1U-10VX-04BR04 PE TXN3 B16
PEG16X RX P4 C592 1 2 .1U-10VX-04BR04 PE TXP4 A15
PEG16X RX N4 C591 1 2 .1U-10VX-04BR04 PE TXN4 B15
PEG16X RX P5 C581 1 2 .1U-10VX-04BR04 PE TXP5 B14
PEG16X RX N5 C582 1 2 .1U-10VX-04BR04 PE TXN5 C14
PEG16X RX P6 C594 1 2 .1U-10VX-04BR04 PE TXP6 A13
PEG16X RX N6 C593 1 2 .1U-10VX-04BR04 PE TXN6 B13
PEG16X RX P7 C579 1 2 .1U-10VX-04BR04 PE TXP7 A12
PEG16X RX N7 C580 1 2 .1U-10VX-04BR04 PE TXN7 B12
PEG16X RX P8 C596 1 2 .1U-10VX-04BR04 PE TXP8 C11
PEG16X RX N8 C595 1 2 .1U-10VX-04BR04 PE TXN8 B11
PEG16X RX P9 C577 1 2 .1U-10VX-04BR04 PE TXP9 A10
PEG16X RX N9 C578 1 2 .1U-10VX-04BR04 PE TXN9 B10
PEG16X RX P10 C598 1 2 .1U-10VX-04BR04 PE TXP10 B9
PEG16X RX N10 C597 1 2 .1U-10VX-04BR04 PE TXN10 C9
PEG16X RX P11 C575 1 2 .1U-10VX-04BR04 PE TXP11 A8
PEG16X RX N11 C576 1 2 .1U-10VX-04BR04 PE TXN11 B8
PEG16X RX P12 C600 1 2 .1U-10VX-04BR04 PE TXP12 A7
PEG16X RX N12 C599 1 2 .1U-10VX-04BR04 PE TXN12 B7
PEG16X RX P13 C573 1 2 .1U-10VX-04BR04 PE TXP13 B6
PEG16X RX N13 C574 1 2 .1U-10VX-04BR04 PE TXN13 C6
PEG16X RX P14 C602 1 2 .1U-10VX-04BR04 PE TXP14 A5
PEG16X RX N14 C601 1 2 .1U-10VX-04BR04 PE TXN14 B5
PEG16X RX P15 C572 1 2 .1U-10VX-04BR04 PE TXP15 A4
PEG16X RX N15 C571 1 2 .1U-10VX-04BR04 PE TXN15 B4

HDAF

US_TXP[0]
US_TXN[0]
US_TXP[1]
US_TXN[1]
US_TXP[2]
US_TXN[2]
US_TXP[3]
US_TXN[3]
US_TXP[4]
US_TXN[4]
US_TXP[5]
US_TXN[5]
US_TXP[6]
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US_TXN[11]
US_TXP[12]
US_TXN[12]
US_TXP[13]
US_TXN[13]
US_TXP[14]
US_TXN[14]
US_TXP[15]
US_TXN[15]

01-201-102720

UPSTREAM TRANSMITTER

UPSTREAM RECEIVER

US_RXP[0] D19 BR04 PE RXP0 SBC33 1 2 .1U-10VX-04-X PEG16X TX P0
US_RXN[0] E19 BR04 PE RXN0 SBC34 1 2 .1U-10VX-04-X PEG16X TX N0
US_RXP[1] D18 BR04 PE RXP1 SBC34 1 2 .1U-10VX-04-X PEG16X TX P1
US_RXN[1] E18 BR04 PE RXN1 SBC35 1 2 .1U-10VX-04-X PEG16X TX N1
US_RXP[2] E17 BR04 PE RXP2 SBC36 1 2 .1U-10VX-04-X PEG16X TX P2
US_RXN[2] D16 BR04 PE RXN2 SBC37 1 2 .1U-10VX-04-X PEG16X TX N2
US_RXP[3] E16 BR04 PE RXP3 SBC38 1 2 .1U-10VX-04-X PEG16X TX P3
US_RXN[3] D15 BR04 PE RXN3 SBC39 1 2 .1U-10VX-04-X PEG16X TX N3
US_RXP[4] D15 BR04 PE RXP4 SBC40 1 2 .1U-10VX-04-X PEG16X TX P4
US_RXN[4] E15 BR04 PE RXN4 SBC41 1 2 .1U-10VX-04-X PEG16X TX N4
US_RXP[5] E14 BR04 PE RXP5 SBC42 1 2 .1U-10VX-04-X PEG16X TX P5
US_RXN[5] D13 BR04 PE RXN5 SBC43 1 2 .1U-10VX-04-X PEG16X TX N5
US_RXP[6] E13 BR04 PE RXP6 SBC44 1 2 .1U-10VX-04-X PEG16X TX P6
US_RXN[6] D12 BR04 PE RXN6 SBC45 1 2 .1U-10VX-04-X PEG16X TX N6
US_RXP[7] D12 BR04 PE RXP7 SBC46 1 2 .1U-10VX-04-X PEG16X TX P7
US_RXN[7] E12 BR04 PE RXN7 SBC47 1 2 .1U-10VX-04-X PEG16X TX N7
US_RXP[8] E11 BR04 PE RXP8 SBC48 1 2 .1U-10VX-04-X PEG16X TX P8
US_RXN[8] D10 BR04 PE RXN8 SBC49 1 2 .1U-10VX-04-X PEG16X TX N8
US_RXP[9] E10 BR04 PE RXP9 SBC50 1 2 .1U-10VX-04-X PEG16X TX P9
US_RXN[9] D9 BR04 PE RXN9 SBC51 1 2 .1U-10VX-04-X PEG16X TX N9
US_RXP[10] E9 BR04 PE RXP10 SBC52 1 2 .1U-10VX-04-X PEG16X TX P10
US_RXN[10] D8 BR04 PE RXN10 SBC53 1 2 .1U-10VX-04-X PEG16X TX N10
US_RXP[11] E8 BR04 PE RXP11 SBC54 1 2 .1U-10VX-04-X PEG16X TX P11
US_RXN[11] D7 BR04 PE RXN11 SBC55 1 2 .1U-10VX-04-X PEG16X TX N11
US_RXP[12] E7 BR04 PE RXP12 SBC56 1 2 .1U-10VX-04-X PEG16X TX P12
US_RXN[12] D6 BR04 PE RXN12 SBC57 1 2 .1U-10VX-04-X PEG16X TX N12
US_RXP[13] E6 BR04 PE RXP13 SBC58 1 2 .1U-10VX-04-X PEG16X TX P13
US_RXN[13] D5 BR04 PE RXN13 SBC59 1 2 .1U-10VX-04-X PEG16X TX N13
US_RXP[14] E5 BR04 PE RXP14 SBC60 1 2 .1U-10VX-04-X PEG16X TX P14
US_RXN[14] D4 BR04 PE RXN14 SBC61 1 2 .1U-10VX-04-X PEG16X TX N14
US_RXP[15] E4 BR04 PE RXP15 SBC62 1 2 .1U-10VX-04-X PEG16X TX P15
US_RXN[15] D3 BR04 PE RXN15 SBC63 1 2 .1U-10VX-04-X PEG16X TX N15

US_RESREF B20 US RESREF 2 ER22 200-1-04

3 PEG_TX_P[0:15] PEG16X TX P[0:15]
3 PEG_TX_N[0:15] PEG16X TX N[0:15]
3 PEG_RX_P[0:15] PEG16X RX P[0:15]
3 PEG_RX_N[0:15] PEG16X RX N[0:15]

Power on Reset

R688 10K-04

R692 10K-04

R689 10K-04

R691 0-04-0

Q21 2N3904-S

Q22 2N3904-S

R690 10K-04

R691 0-04-0

R692 10K-04

R693 10K-04

R694 10K-04

R695 10K-04

R696 10K-04

R697 10K-04

R698 10K-04

R699 10K-04

R700 10K-04

R701 10K-04

R702 10K-04

R703 10K-04

R704 10K-04

R705 10K-04

R706 10K-04

R707 10K-04

R708 10K-04

R709 10K-04

R710 10K-04

R711 10K-04

R712 10K-04

R713 10K-04

R714 10K-04

I2C_mode pin="0" reflects I2C mode.
I2C_mode pin="1" reflects SMBUS mode.

Elitegroup Computer Systems





SLI - LUCID LT24102 US

Document Number P67H2-A





Date: Wednesday, September 15, 2010 Sheet 15 of 42

External Connection





PCIe16X_1

17	PE16X_RX_P[0:15]		PE16X_RX_P[0:15]
17	PE16X_RX_N[0:15]		PE16X_RX_N[0:15]
17	PE16X_TX_P[0:15]		PE16X_TX_P[0:15]
17	PE16X_TX_N[0:15]		PE16X_TX_N[0:15]

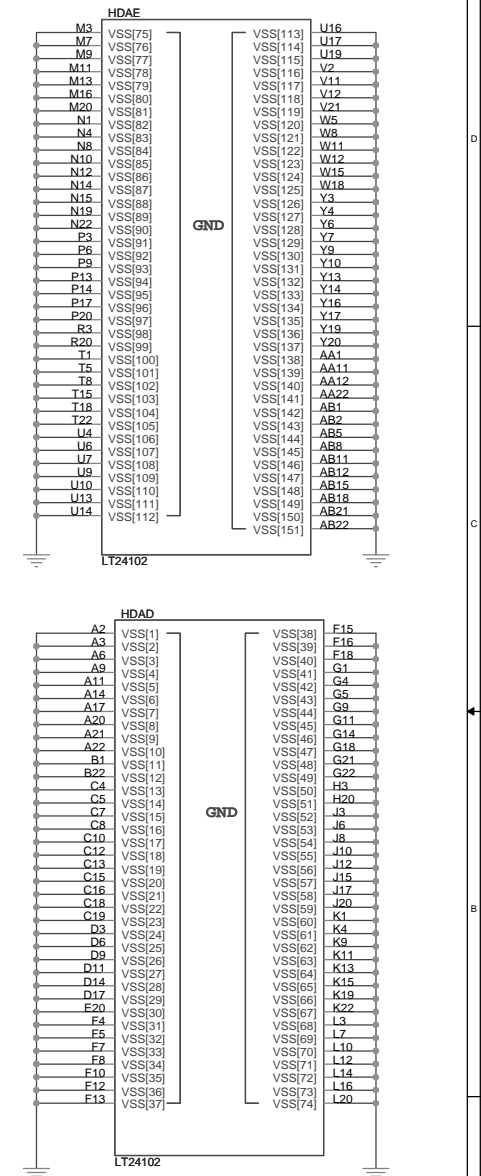
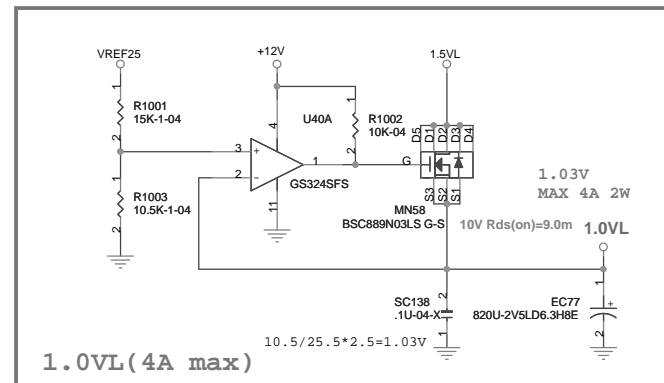
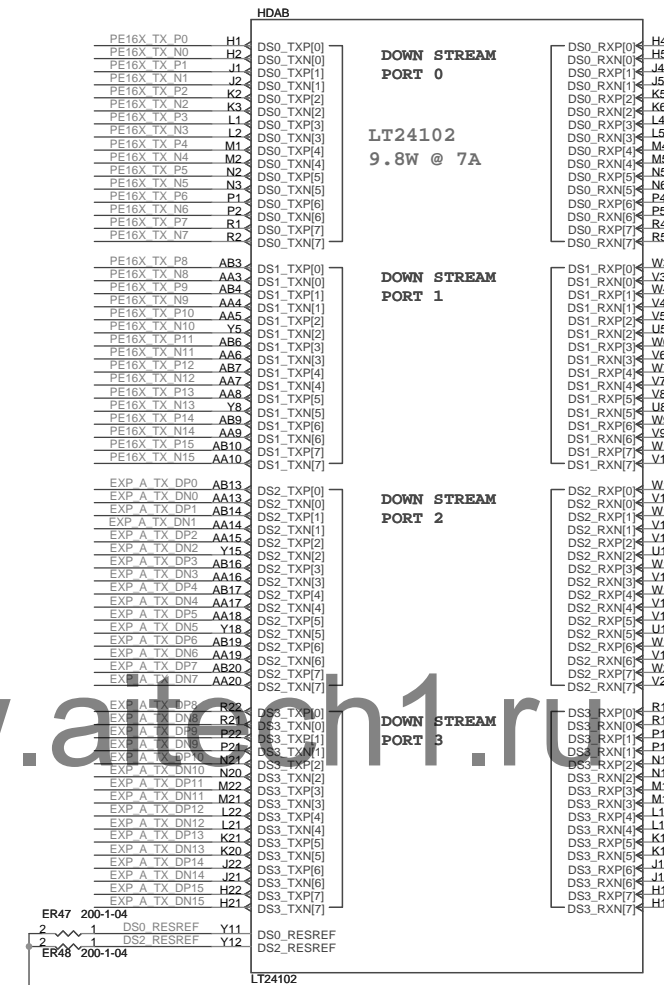
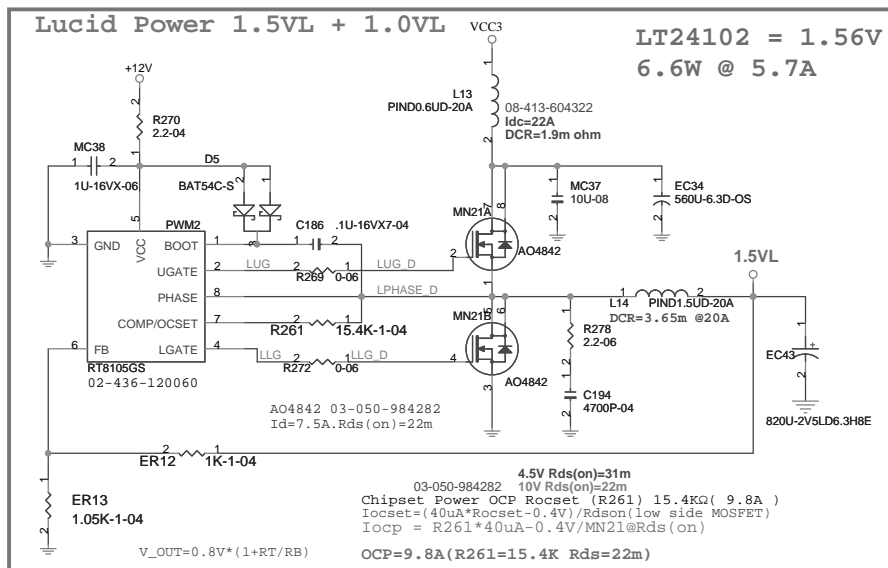
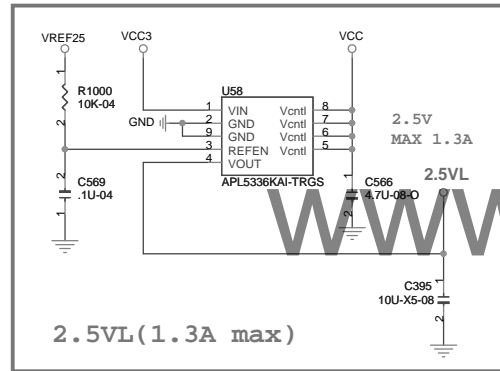
PCIe16X_2

18	EXP_A_RX_DP[0..7]		EXP_A_RX_DP[0..7]
18	EXP_A_RX_DN[0..7]		EXP_A_RX_DN[0..7]
18	EXP_A_TX_DP[0..7]		EXP_A_TX_DP[0..7]
18	EXP_A_TX_DN[0..7]		EXP_A_TX_DN[0..7]

PCIe16X_3

19	EXP_A_RX_DP[8..15]		EXP_A_RX_DP[8..15]
19	EXP_A_RX_DN[8..15]		EXP_A_RX_DN[8..15]
19	EXP_A_TX_DP[8..15]		EXP_A_TX_DP[8..15]
19	EXP_A_TX_DN[8..15]		EXP_A_TX_DN[8..15]

48 x 5 Gbps SERDES lanes,
a full PCI-Express switch with
one x16 upstream port,
two x16 downstream ports
and an embedded end point.



11,18,19,27,28,29,30,31,33 PCIE_WAKE_L << PCIE_WAKE_L
7,8,11,15,18,19,35,39 SMBCLK >> SMBCLK
7,8,11,15,18,19,35,39 SMBDATA << SMBDATA

15,18,19,24,33 SIO_PCIE16X1_L >> PEX16_RST_L

16 PE16X_RX_P[0:15] << PE16X_RX_P[0:15]
16 PE16X_RX_N[0:15] << PE16X_RX_N[0:15]
16 PE16X_TX_P[0:15] >> PE16X_TX_P[0:15]
16 PE16X_TX_N[0:15] >> PE16X_TX_N[0:15]

12 CK_PE_BUF_P >> CK_PE_BUF_P
12 CK_PE_BUF_N >> CK_PE_BUF_N

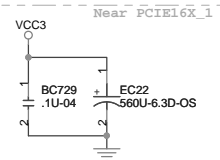
15 CK_NF200P >> CK_NF200P
15 CK_NF200N >> CK_NF200N

18 CK_PE16X_2P >> CK_PE16X_2P
18 CK_PE16X_2N >> CK_PE16X_2N

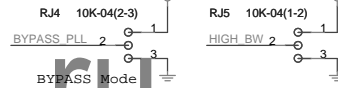
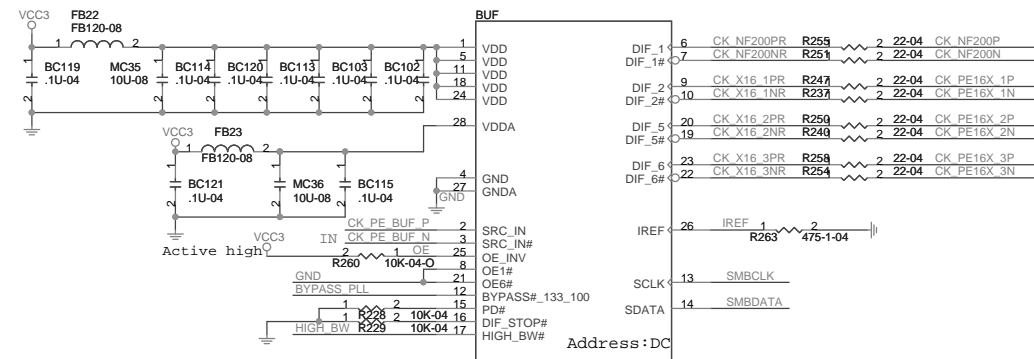
19 CK_PE16X_3P >> CK_PE16X_3P
19 CK_PE16X_3N >> CK_PE16X_3N

PE16X_TX_CP0 BC89 1 2 .1U-10VX-04 16X TX P0
PE16X_TX_CP1 BC92 1 2 .1U-10VX-04 16X TX P1
PE16X_TX_CP2 BC96 1 2 .1U-10VX-04 16X TX P2
PE16X_TX_CP3 BC101 1 2 .1U-10VX-04 16X TX P3
PE16X_TX_CP4 BC112 1 2 .1U-10VX-04 16X TX P4
PE16X_TX_CP5 BC118 1 2 .1U-10VX-04 16X TX P5
PE16X_TX_CP6 BC128 1 2 .1U-10VX-04 16X TX P6
PE16X_TX_CP7 BC132 1 2 .1U-10VX-04 16X TX P7
PE16X_TX_CP8 BC136 1 2 .1U-10VX-04 16X TX P8
PE16X_TX_CP9 BC139 1 2 .1U-10VX-04 16X TX P9
PE16X_TX_CP10 BC143 1 2 .1U-10VX-04 16X TX P10
PE16X_TX_CP11 BC154 1 2 .1U-10VX-04 16X TX P11
PE16X_TX_CP12 BC161 1 2 .1U-10VX-04 16X TX P12
PE16X_TX_CP13 BC170 1 2 .1U-10VX-04 16X TX P13
PE16X_TX_CP14 BC181 1 2 .1U-10VX-04 16X TX P14
PE16X_TX_CP15 BC191 1 2 .1U-10VX-04 16X TX P15

PE16X_TX_CN0 BC87 1 2 .1U-10VX-04 16X TX N0
PE16X_TX_CN1 BC93 1 2 .1U-10VX-04 16X TX N1
PE16X_TX_CN2 BC98 1 2 .1U-10VX-04 16X TX N2
PE16X_TX_CN3 BC104 1 2 .1U-10VX-04 16X TX N3
PE16X_TX_CN4 BC110 1 2 .1U-10VX-04 16X TX N4
PE16X_TX_CN5 BC123 1 2 .1U-10VX-04 16X TX N5
PE16X_TX_CN6 BC126 1 2 .1U-10VX-04 16X TX N6
PE16X_TX_CN7 BC134 1 2 .1U-10VX-04 16X TX N7
PE16X_TX_CN8 BC137 1 2 .1U-10VX-04 16X TX N8
PE16X_TX_CN9 BC140 1 2 .1U-10VX-04 16X TX N9
PE16X_TX_CN10 BC146 1 2 .1U-10VX-04 16X TX N10
PE16X_TX_CN11 BC157 1 2 .1U-10VX-04 16X TX N11
PE16X_TX_CN12 BC163 1 2 .1U-10VX-04 16X TX N12
PE16X_TX_CN13 BC173 1 2 .1U-10VX-04 16X TX N13
PE16X_TX_CN14 BC185 1 2 .1U-10VX-04 16X TX N14
PE16X_TX_CN15 BC193 1 2 .1U-10VX-04 16X TX N15



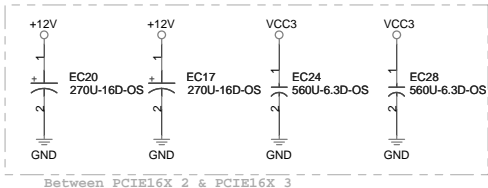
Clock ZDB ICS9DB403



CK_NF200P R259 2 49.9-1-04
CK_NF200N R252 2 49.9-1-04
CK_PE16X_1P R249 2 49.9-1-04
CK_PE16X_1N R238 2 49.9-1-04
CK_PE16X_2P R249 2 49.9-1-04
CK_PE16X_2N R239 2 49.9-1-04
CK_PE16X_3P R251 2 49.9-1-04
CK_PE16X_3N R253 2 49.9-1-04

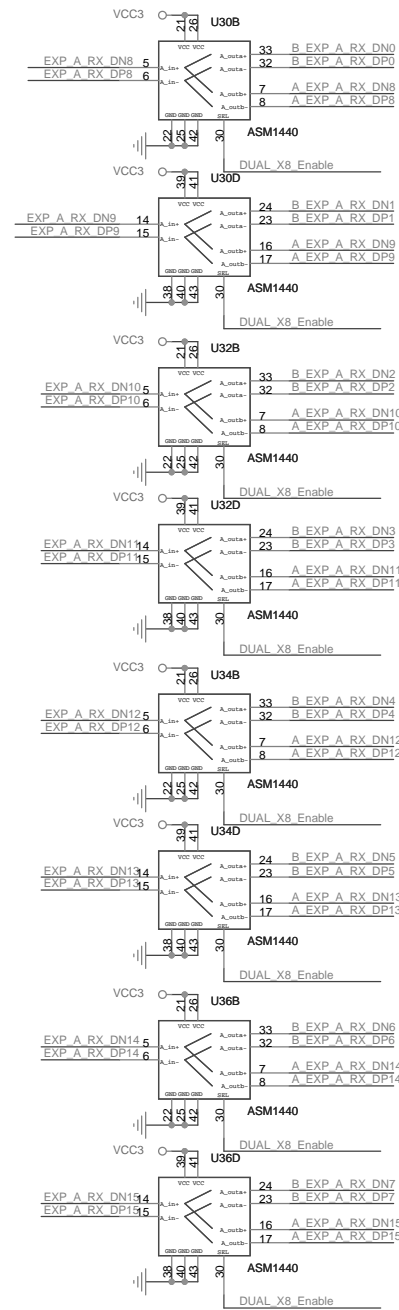
External Connection

16 EXP_A_TX_DN[8..15]	└─	EXP A TX DN[8..15]
16 EXP_A_TX_DP[8..15]	└─	EXP A TX DP[8..15]
16 EXP_A_RX_DN[8..15]	└─	EXP A RX DN[8..15]
16 EXP_A_RX_DP[8..15]	└─	EXP A RX DP[8..15]
18 A_EXP_A_TX_DN[8..15]	└─	A EXP A TX DN[8..15]
18 A_EXP_A_TX_DP[8..15]	└─	A EXP A TX DP[8..15]
18 A_EXP_A_RX_DN[8..15]	└─	A EXP A RX DN[8..15]
18 A_EXP_A_RX_DP[8..15]	└─	A EXP A RX DP[8..15]
17 CK_1P16X_3N	└─	CK 16P B DN
17 CK_1P16X_3P	└─	CK 16P B DP
15,17,18,24,33 SIO_PCIRST1_L	└─	PEX16_RST_L
11,17,18,27,28,29,30,31,33 PCIE_WAKE_L	└─	PCIE_WAKE_L
7,8,11,15,17,18,35,39 SMBCLK	└─	SMBCLK
7,8,11,15,17,18,35,39 SMBDATA	└─	SMBDATA
15 EXP_B_PRSENT_L	└─	DUAL X8 Enable



B EXP A TXP 7 C BC131	1	2	.1U-10VX-04	EXP A TX DP7
B EXP A TXN 7 C BC133	1	2	.1U-10VX-04	EXP A TX DN7

B EXP A TXP 7 C BC131	1	2	.1U-10VX-04	EXP A TX DP7
B EXP A TXN 7 C BC133	1	2	.1U-10VX-04	EXP A TX DN7



VCC3

BC124 1.0U-04

BC108 1.0U-04

BC105 1.0U-04

BC141 1.0U-04

BC138 1.0U-04

BC129 1.0U-04

BC171 1.0U-04

BC153 1.0U-04

BC145 1.0U-04

BC197 1.0U-04

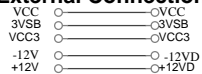
BC207 1.0U-04

BC151 1.0U-04

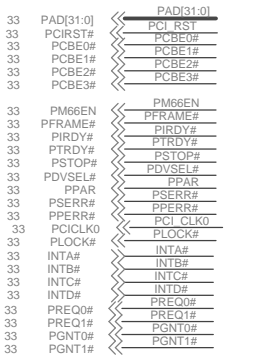
ASM1440 bypass Cap

每組三顆

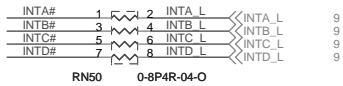
External Connection



COMMON

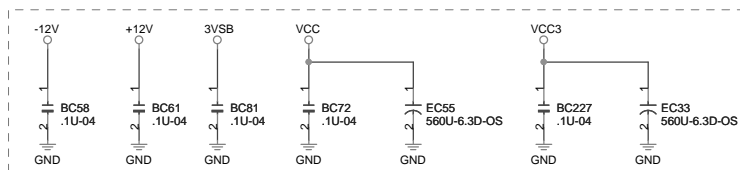
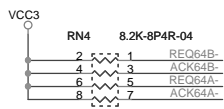
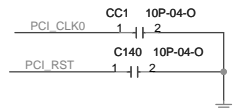
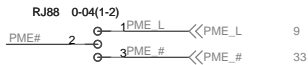


PCI slot PCH

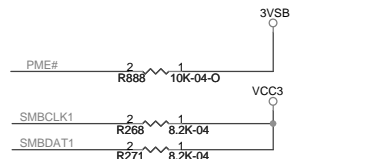


PCI CHIP

PCI Slot:
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/S0/3.75A



PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD

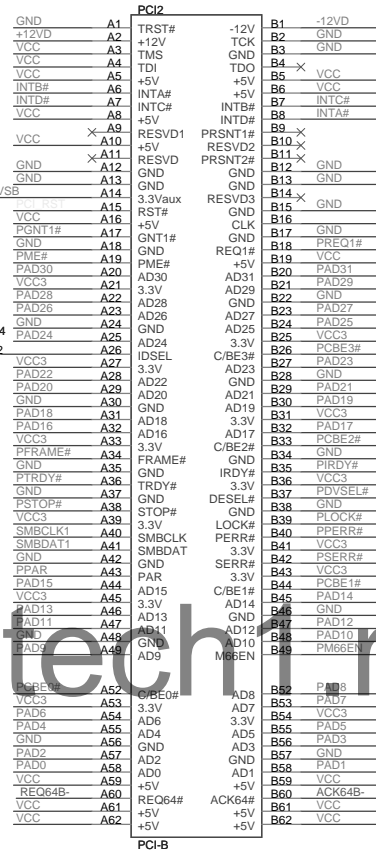


PCI1



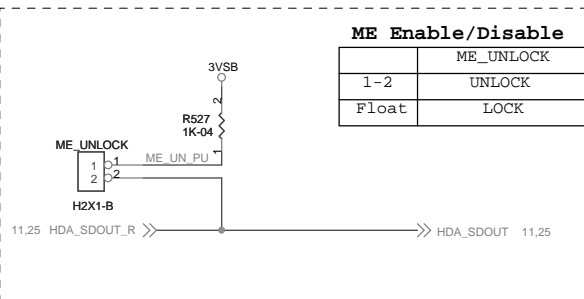
PCI-B

PCI2

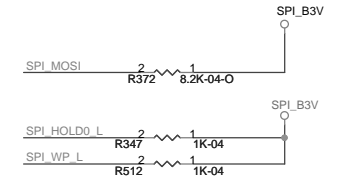
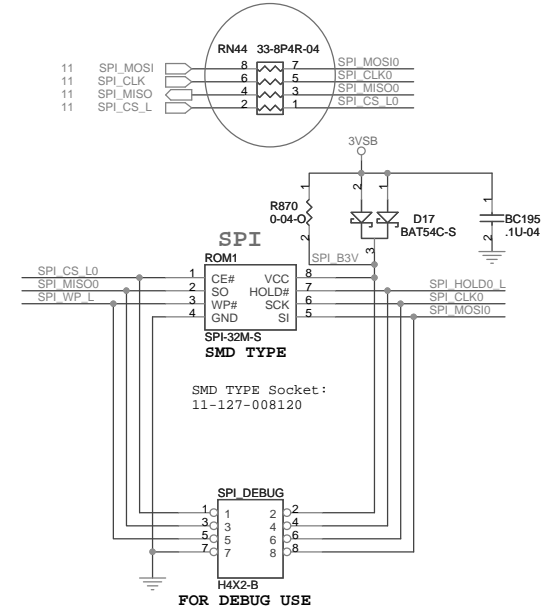


ME Enable/Disable

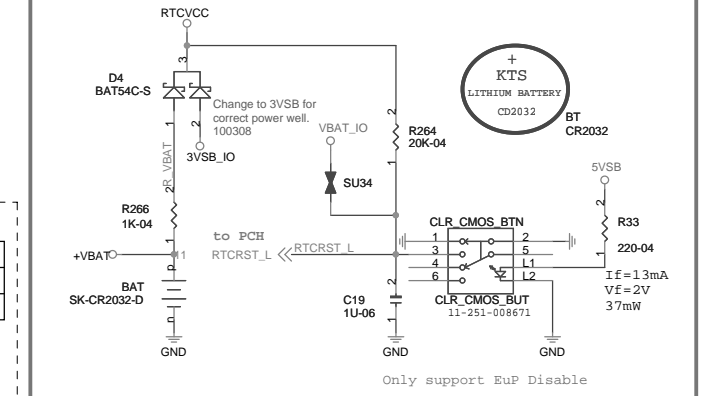
	ME_UNLOCK
1-2	UNLOCK
Float	LOCK



SPI ROM Circuit



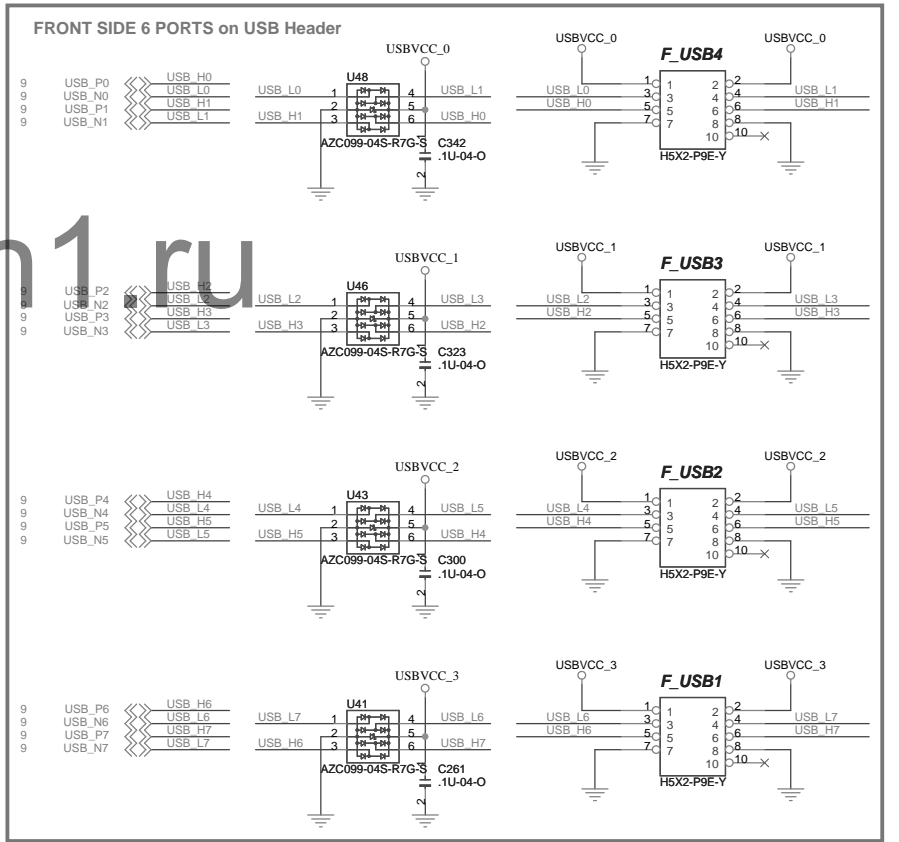
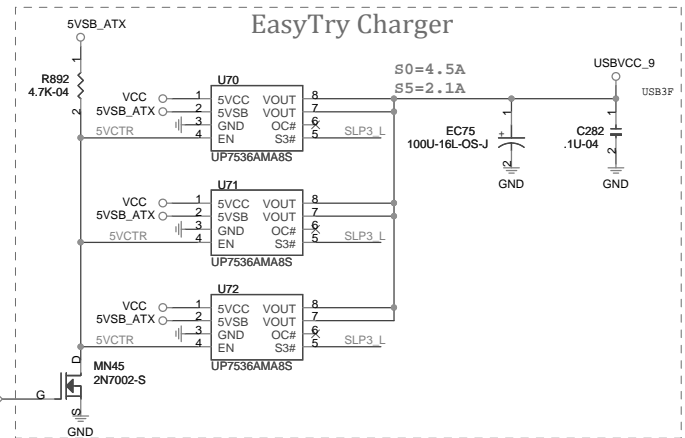
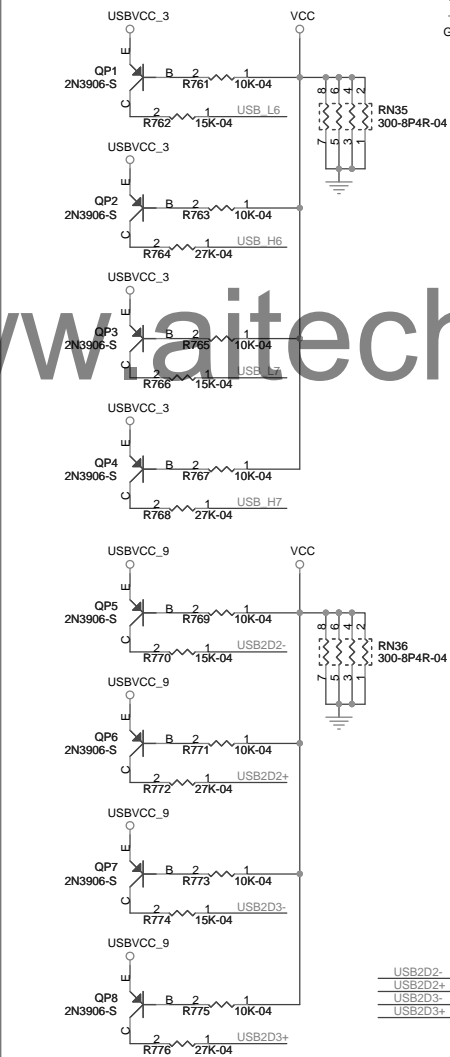
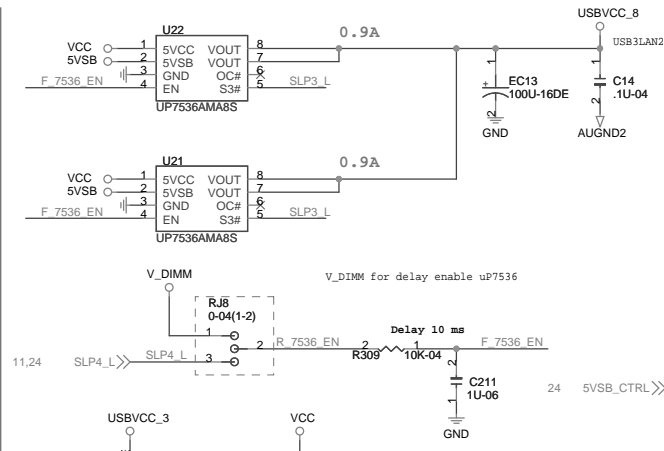
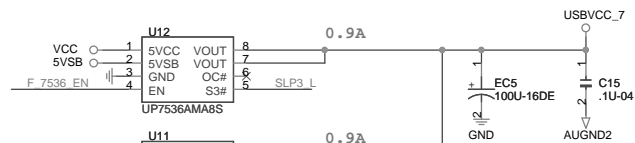
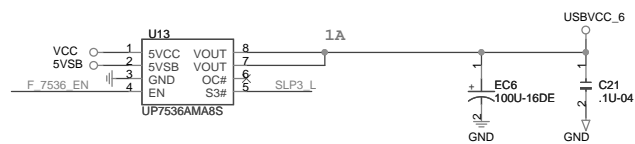
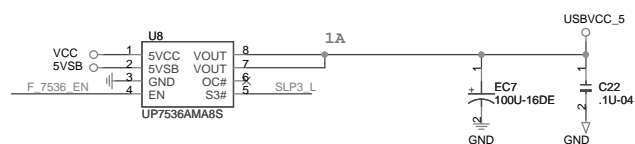
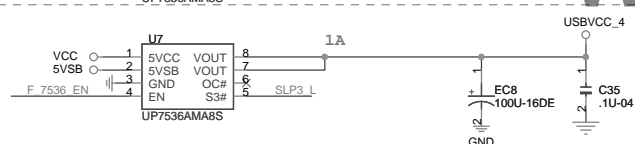
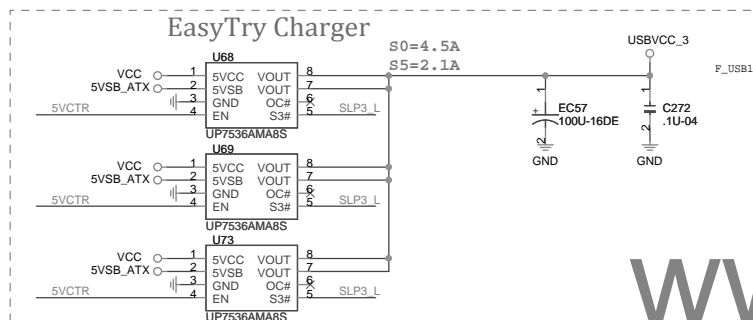
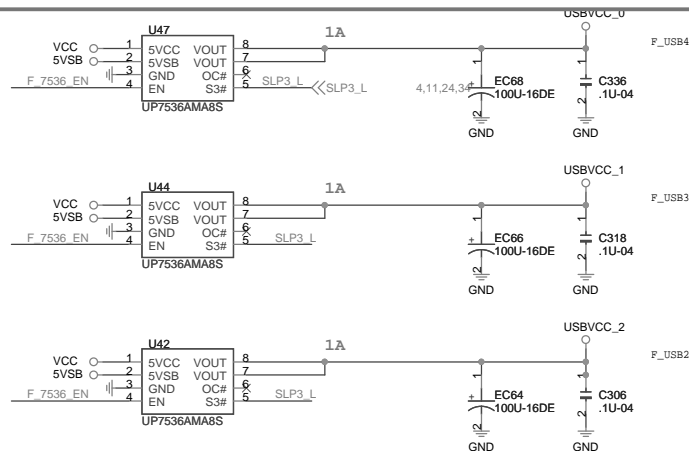
CLR CMOS Button / STBY LED

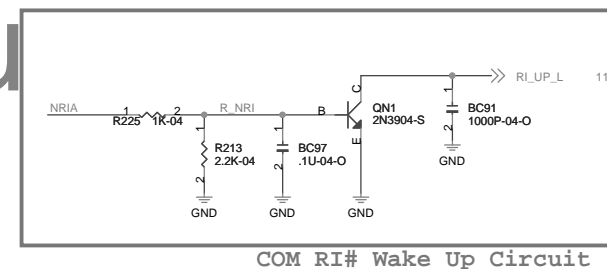
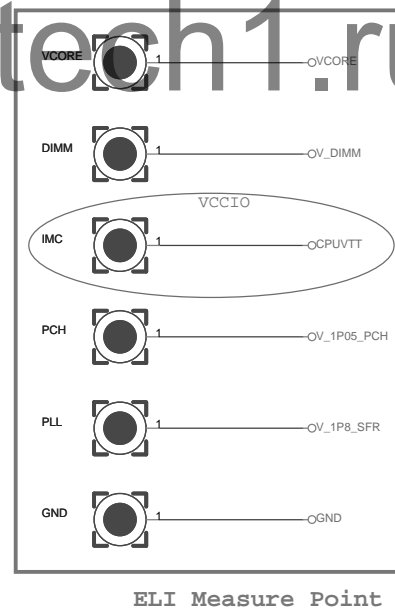
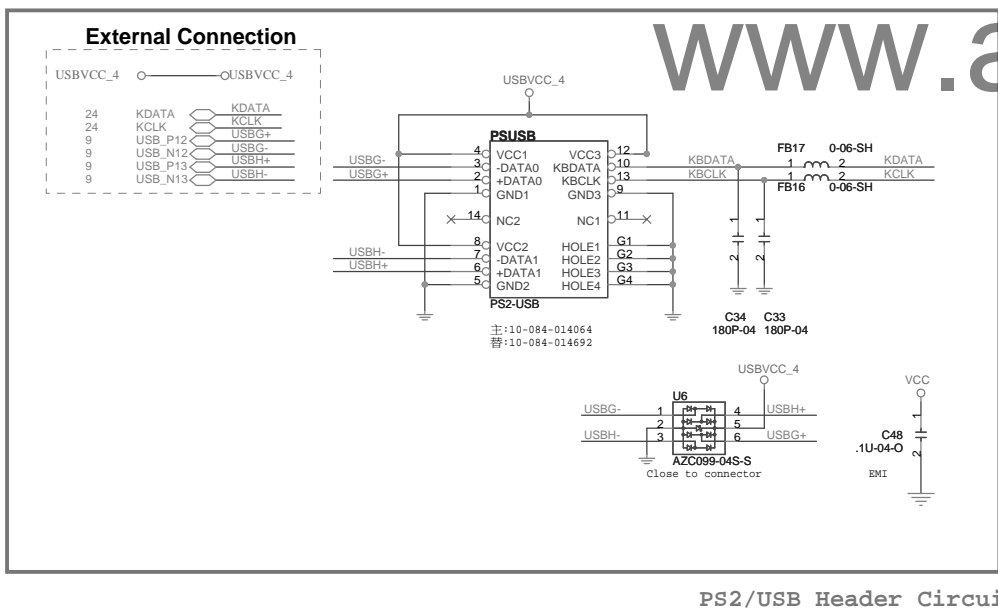
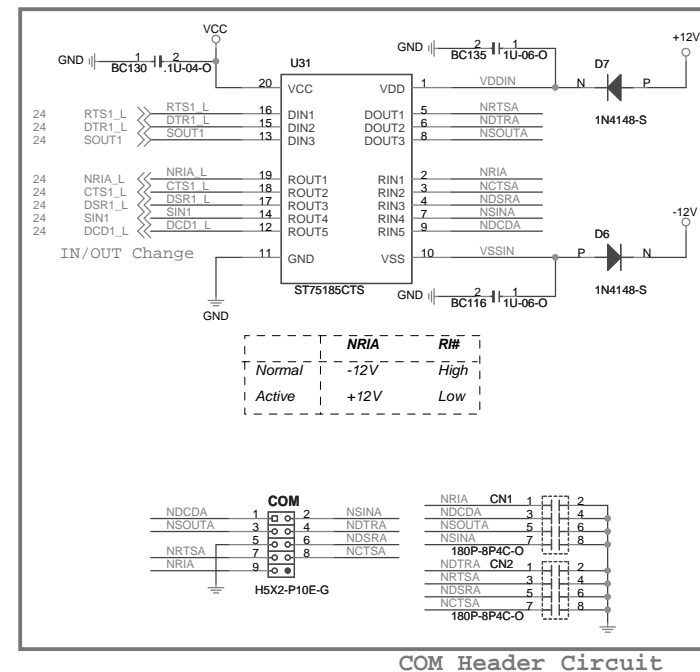
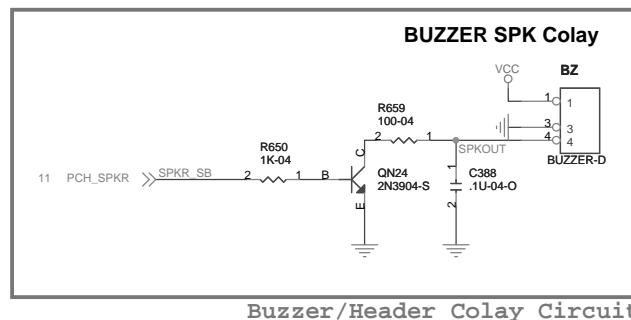
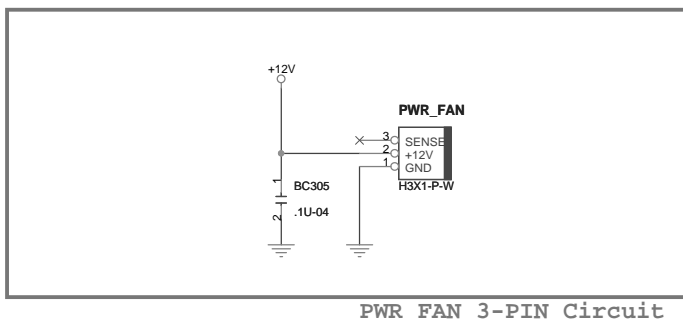
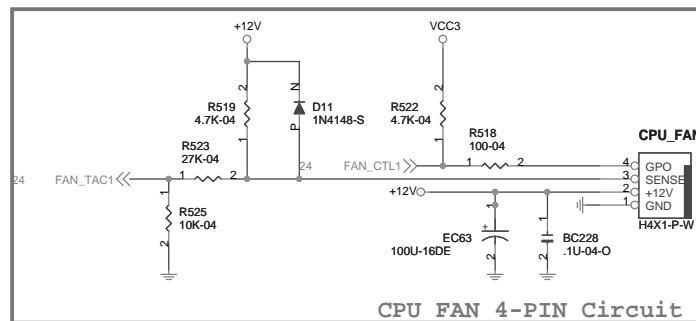
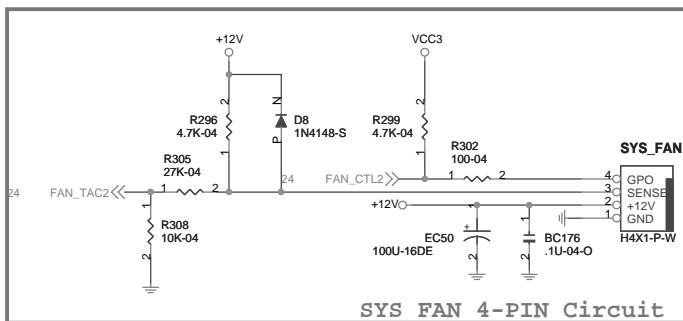


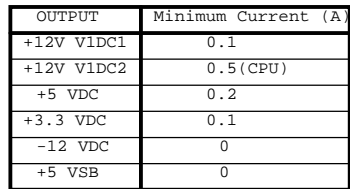
Elitegroup Computer Systems

Title			SLOT - PCI, SPI, CLR_CMOS
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Custom			
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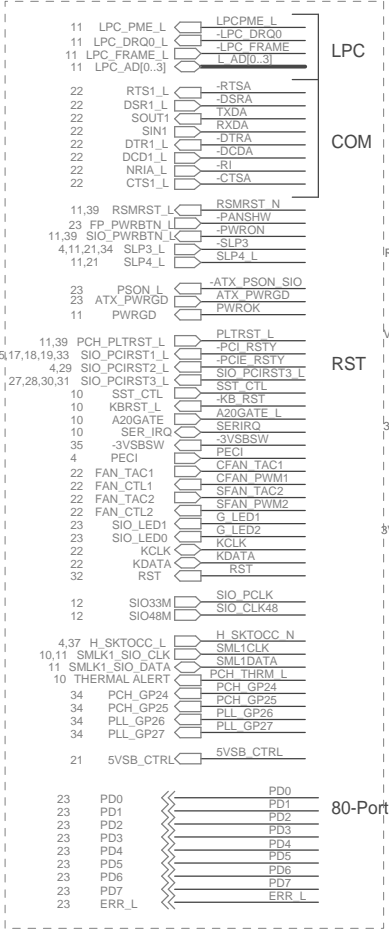
USB POWER CIRCUIT.







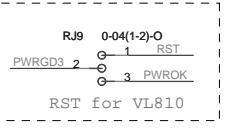
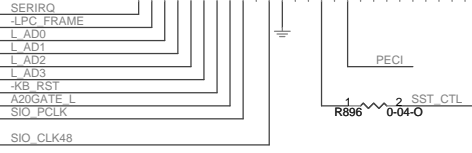
External Connection



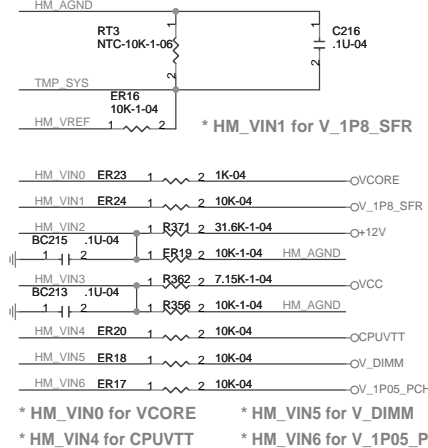
HW STRAPPING

JP2 Pin122	WDT_EN	Disable WDT to reset PWROK
JP4 Pin126	K8PWR_EN	Enable WDT to reset PWROK
JP5 Pin46	FAN_CTL_SEL	K8 power sequence function is disabled
JP6 Pin72	RSMRST_SEL	The default value of EC Index 63h/6Bh/73h is 80h
		The default value of EC Index 63h/6Bh/73h is FFh
		The default value of EC Index 63h/6Bh/73h is 00h
		The default value of EC Index 63h/6Bh/73h is 40h
		RSMRST# output detected by 3VSB
		Enable WDT to reset PWROK

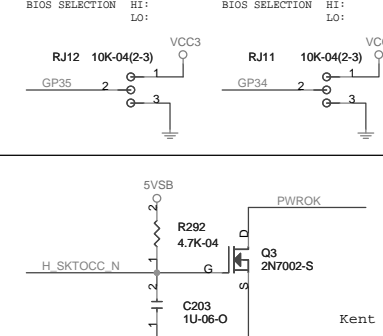
SIO_PCIRST1_L : NF200 + PCIE1 + PCIE2 + PCI
SIO_PCIRST2_L : CPU + eSATA
SIO_PCIRST3_L : LANx2 + USBx2



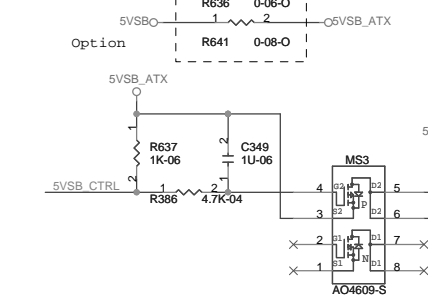
Thermal and Voltage Monitor



BIOS SELECTION

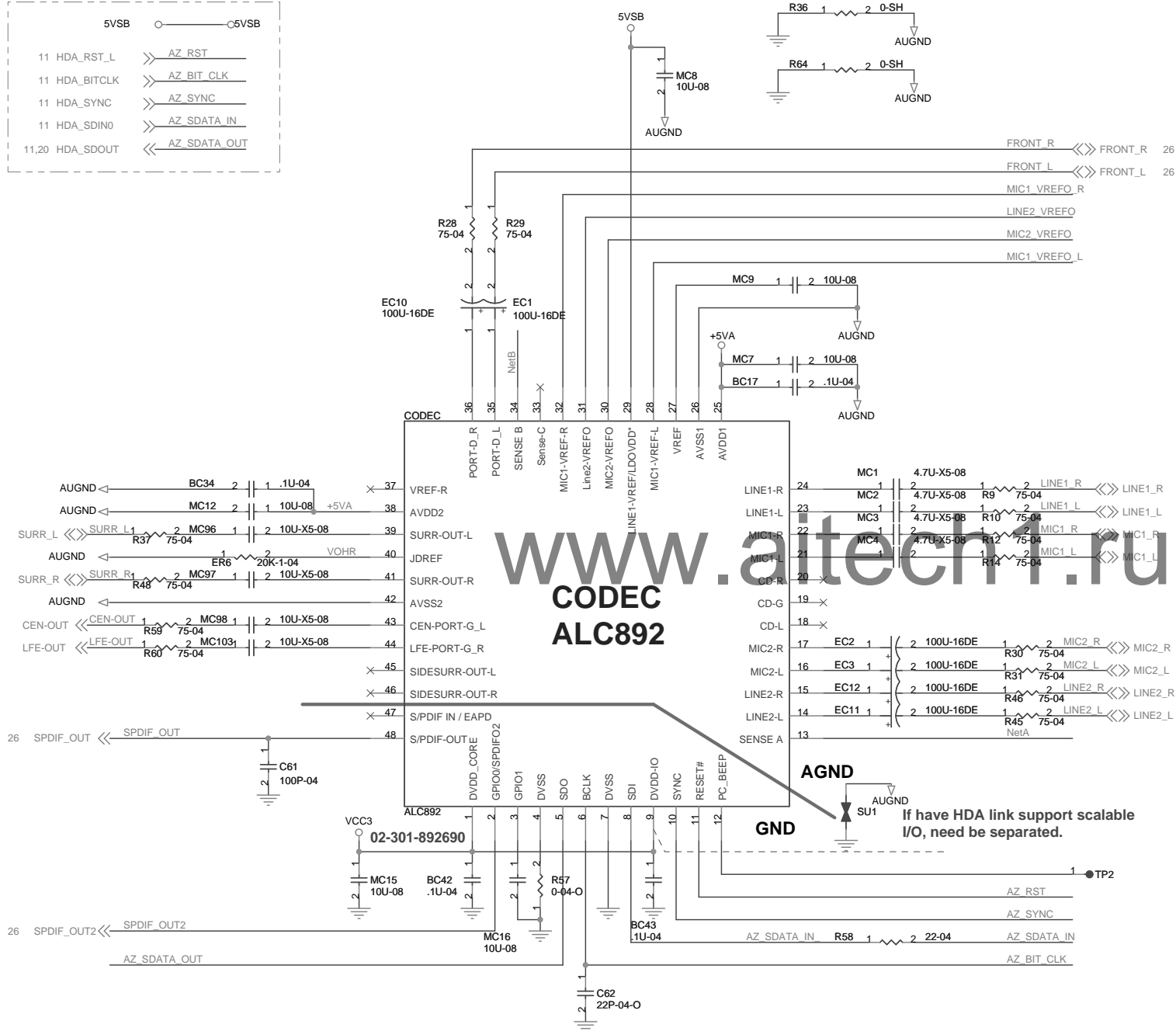
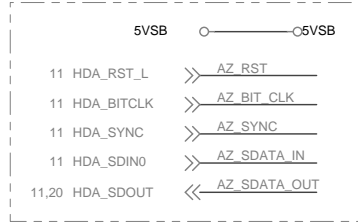


EuP

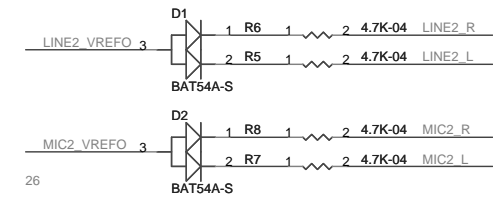
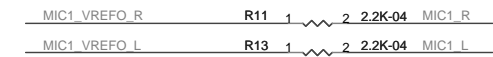


SIO - ITE8728		
Size	Document Number	Rev
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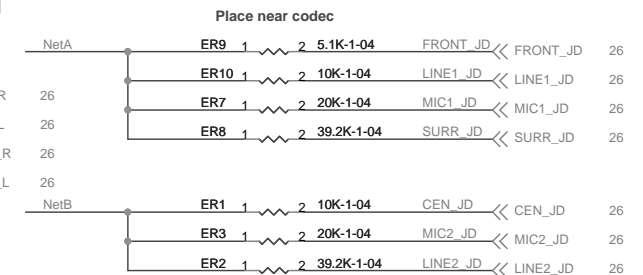
External Connection



Verfourt bias for stereo microphone.



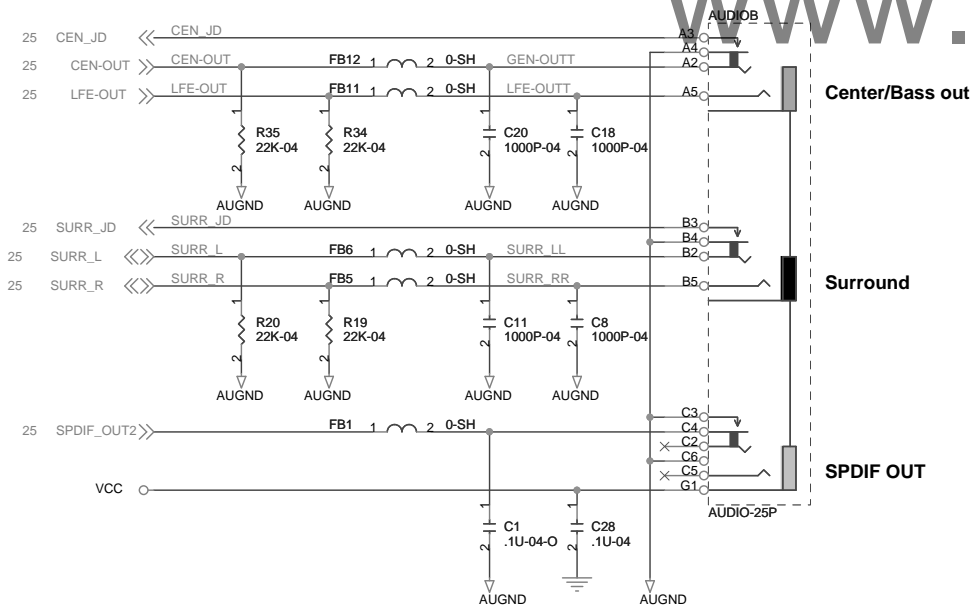
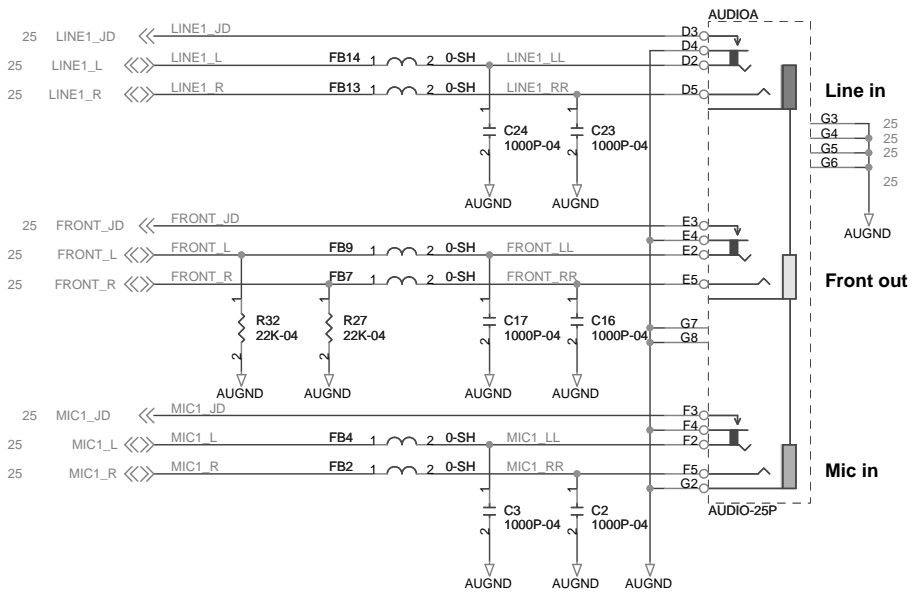
Resistors Networks



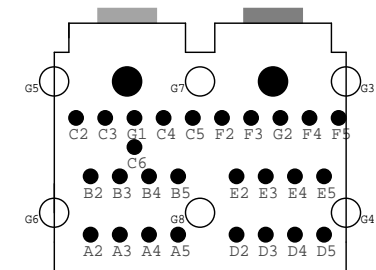
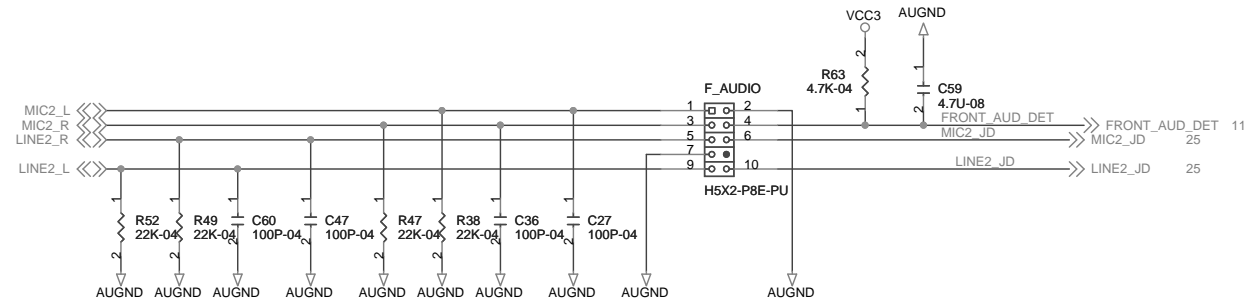
Elitegroup Computer Systems

Title		AUDIO - ALC892(CHIP)	
Size	Document Number	P67H2-A	
Custom		Rev 1.1	
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REAR AUDIO

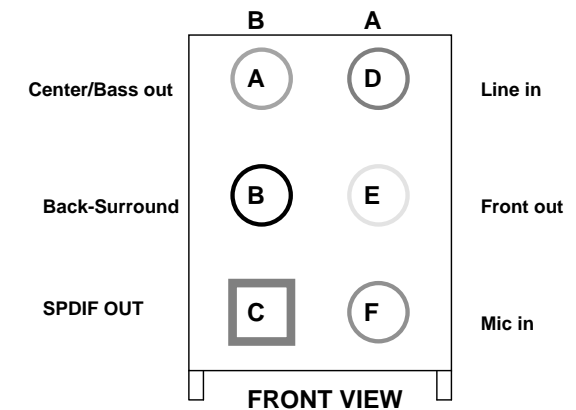
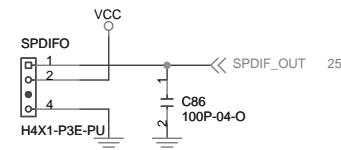


FRONT AUDIO



TOP VIEW

SPDIF OUT



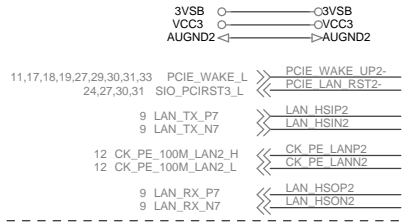
Elitegroup Computer Systems

Title	AUDIO - ALC892(PANEL)
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Size Custom	Document Number P67H2-A	Rev 1.1
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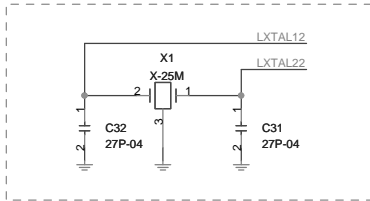
Date: Wednesday, September 15, 2010 Sheet 26 of 42

External Connection

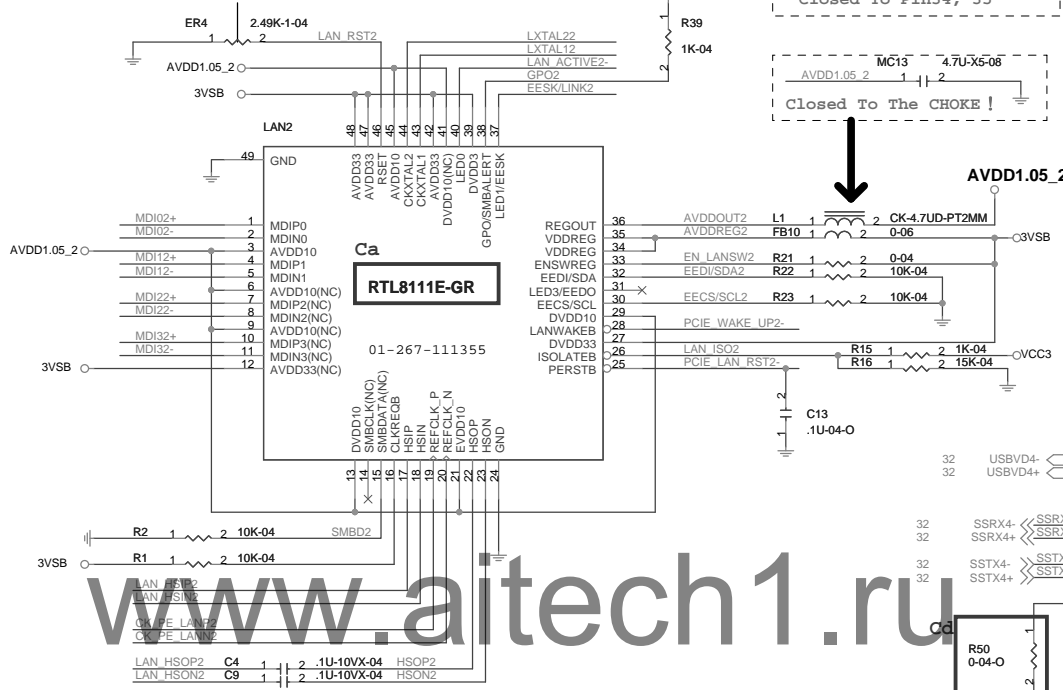


新手提醒:

LAN_HSOP/N請接到SB的PCIE RX端
 LAN_HSI2/N請接到SB的PCIE TX端
 LAN_HSI2/N在SB的PCIE TX端要記得放AC coupling cap

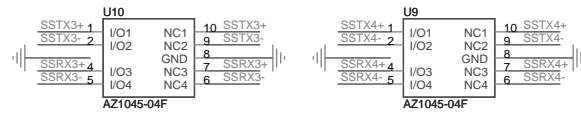


Closed to LAN & trace need GND shielding

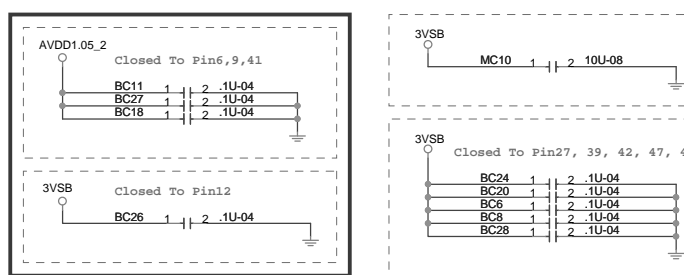


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Low-P ESD for High Speed & EYE-Pattern

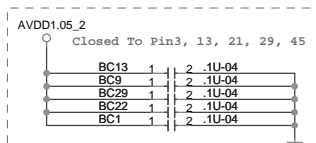
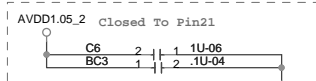
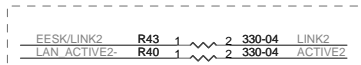
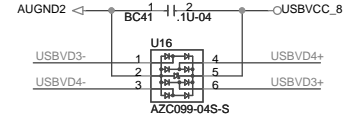
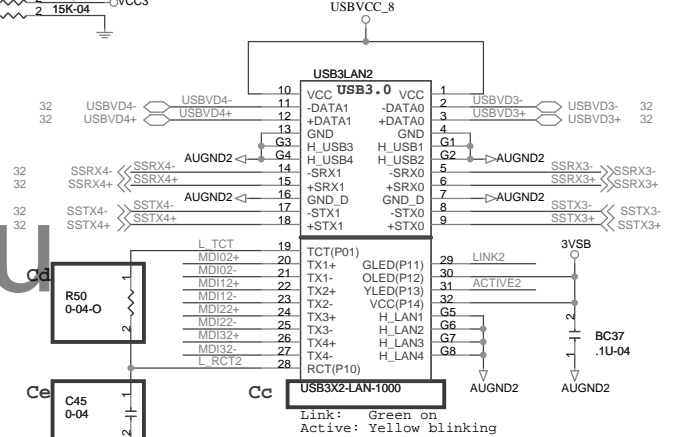
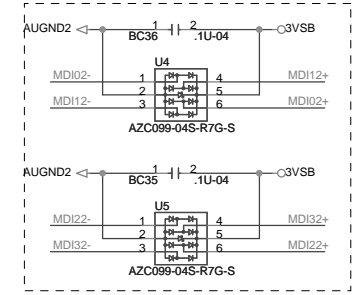


Cb

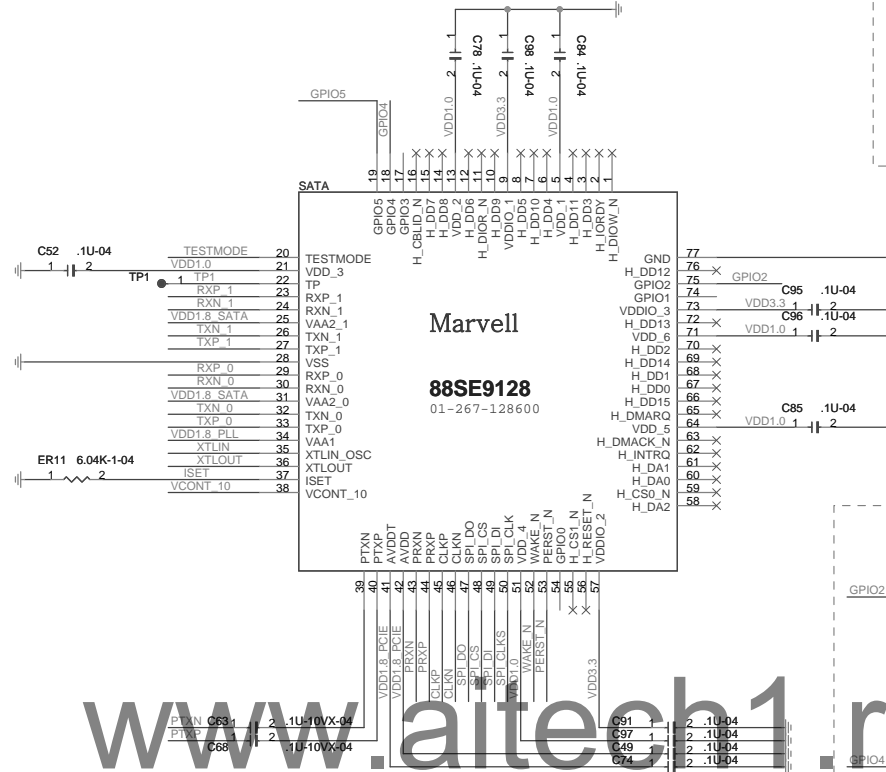
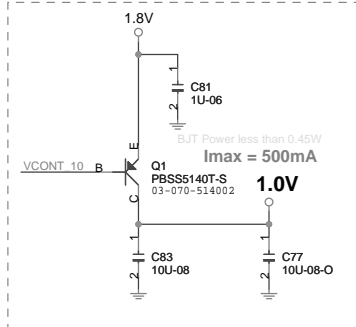
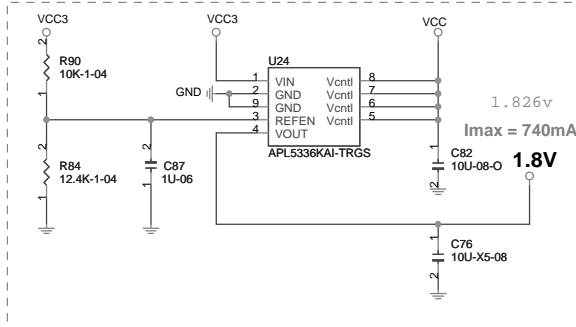
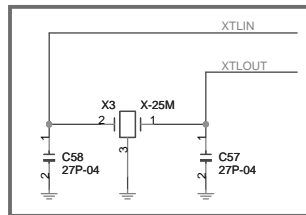
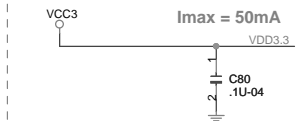
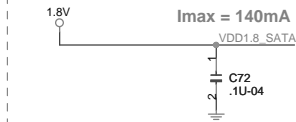
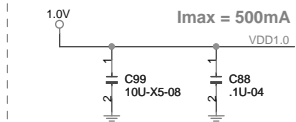
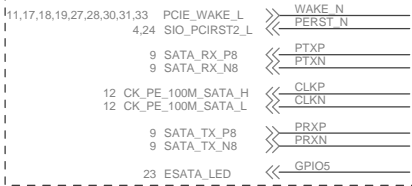


BOM Difference

	RTL8111E-GR 1000M	RTL8105E-GR 10/100M
Ca	RTL8111E-GR	RTL8105E-GR
Cb	V	X
Cc	USBX2-LAN-1000	USBX2-LAN-100
Cd	X	V
Ce	0-04	.01U-04
Cf		
Cg		

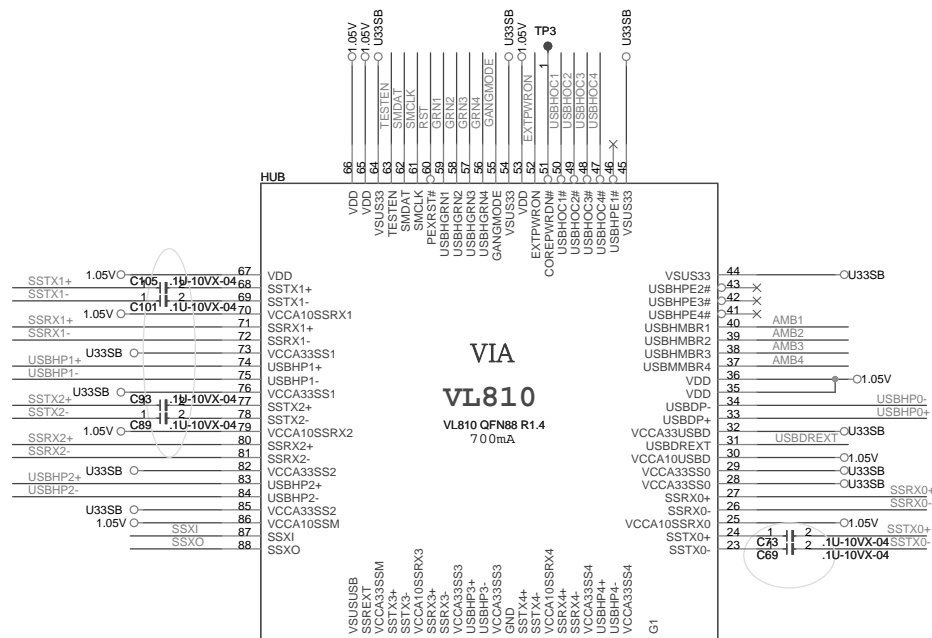


External Connection

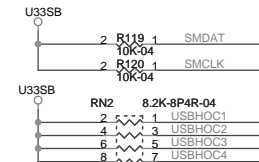
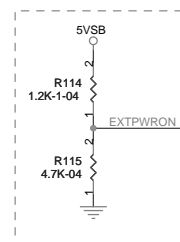
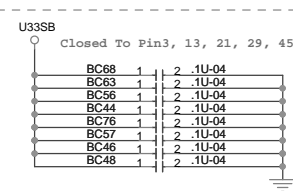
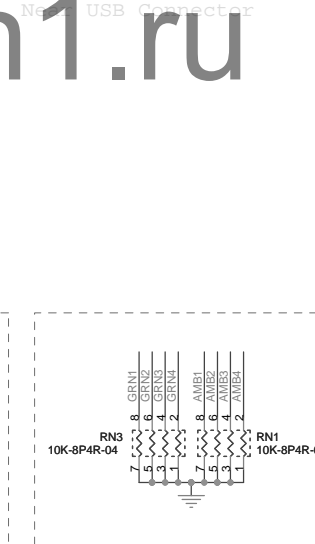
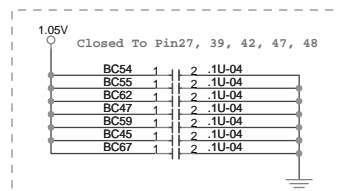
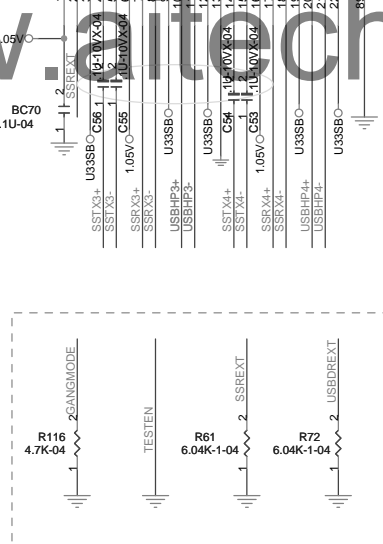
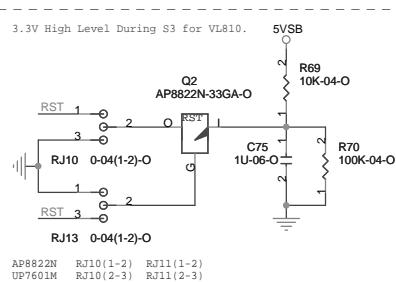
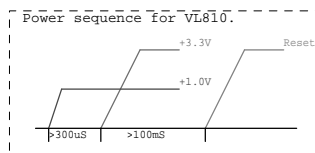
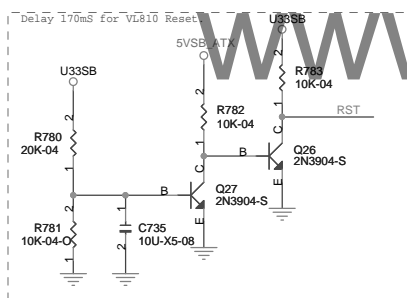
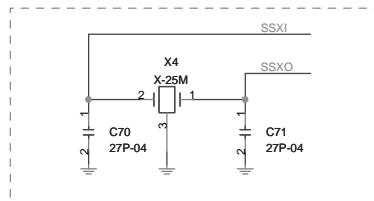


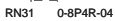
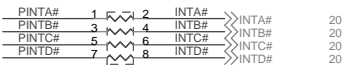
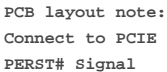
External Connection

24	RST	»	RST	_____
30	+SRX0	»	SSTX0+	_____
30	-SRX0	»	SSTX0-	_____
30	+STX0	»	SSRX0+	_____
30	-STX0	»	SSRX0-	_____
30	USB2D0+	»	USBHP0+	_____
30	USB2D0-	»	USBHP0-	_____
27	SSTX1+	»	SSTX1+	_____
27	SSTX1-	»	SSTX1-	_____
27	SSRX1+	»	SSRX1+	_____
27	SSRX1-	»	SSRX1-	_____
27	USBV1D+	»	USBHP1+	_____
27	USBV1D-	»	USBHP1-	_____
27	SSTX2+	»	SSTX2+	_____
27	SSTX2-	»	SSTX2-	_____
27	SSRX2+	»	SSRX2+	_____
27	SSRX2-	»	SSRX2-	_____
27	USBV2D+	»	USBHP2+	_____
27	USBV2D-	»	USBHP2-	_____
28	SSTX3+	»	SSTX3+	_____
28	SSTX3-	»	SSTX3-	_____
28	SSRX3+	»	SSRX3+	_____
28	SSRX3-	»	SSRX3-	_____
28	USBV3+	»	USBHP3+	_____
28	USBV3-	»	USBHP3-	_____
28	SSTX4+	»	SSTX4+	_____
28	SSTX4-	»	SSTX4-	_____
28	SSRX4+	»	SSRX4+	_____
28	SSRX4-	»	SSRX4-	_____
28	USBV4D+	»	USBHP4+	_____
28	USBV4D-	»	USBHP4-	_____

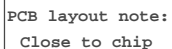
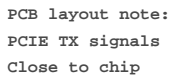
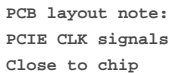


LAN_HSOP/N請接到SB的PCIE RX端
LAN_HSIP/N請接到SB的PCIE TX端





PCB layout note:
PCIE CLK signals
Close to Chip



PCIE DIP;DIN;DOP;DON PCB layout note:

- o meet Differential Impedance : 85 ohm +/- 15%
- o meet Single-ended Impedance : 50 ohm +/- 15%

PCIE DIP and DIN trace width:9.5 mils

PCIE DOP and DON trace width:9.5 mils

Space between DIP/DIN and DOP/DON:14.5 mils

L1 & L2 height:5 mils

The signal traces Number of vias: 2 (Max.)

The signal trace above analog GND plane

Spacing from other groups:>25 mils

Total trace length: 12 inches (Max.)

PCIE CLK PCB layout note:

To meet Differential Impedance :100 ohm +/- 15%

To meet Single-ended Impedance :50 ohm +/- 15%

CLKP and CLKN trace width:7 mils

Space between CLKP and CLKN:14 mils

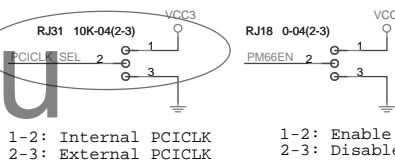
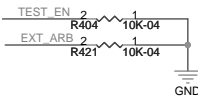
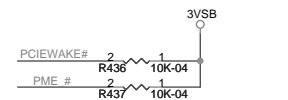
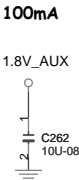
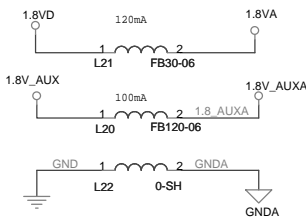
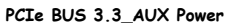
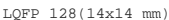
L1 & L2 height:5 mils

The signal traces Number of vias: 4 (Max.)

The signal trace above analog GND plane

Spacing from other groups:>25 mils

Total trace length: 12 inches (Max.)



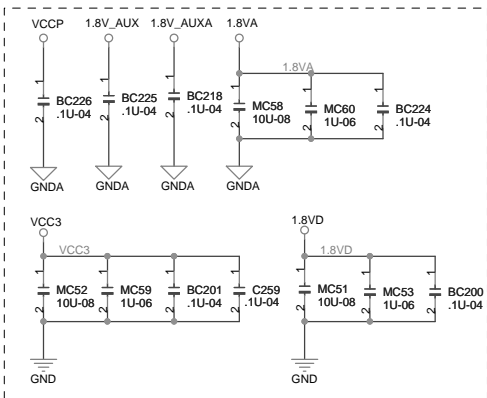
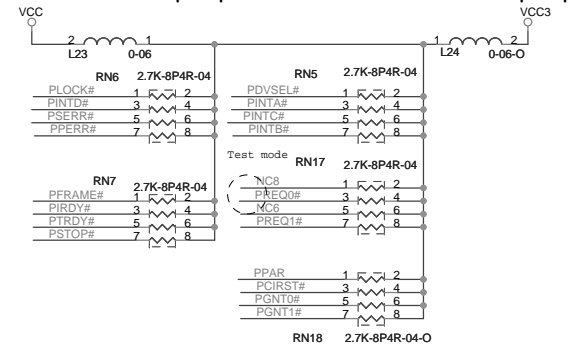
1-2: Internal PCICLK
2-3: External PCICLK

```
1-2: Enable
2-3: Disable
```

```
1-2: PERST#
2-3: POR
```

PCI BUS 5V external pull up

PCI BUS 3.3V external pull up



Elitegroup Computer Systems

Title	Author	Year	Source
1. The Role of the Teacher in the 21st Century	John Hattie	2009	Visible Learning
2. The Power of Learning Styles	David P. Feldman	2008	Learning Styles
3. The Importance of Formative Assessment	Black & Wiliam	1998	Assessment in Education
4. The Impact of Classroom Management	Robert Marzano	2007	The Art and Science of Classroom Management
5. The Role of Technology in Education	Mark Prensky	2001	The Future of Learning
6. The Importance of Social-Emotional Learning	Debra L. Sawyer	2010	Social-Emotional Learning
7. The Role of Parental Involvement	John Hattie	2009	Visible Learning
8. The Impact of Differentiated Instruction	Carol Ann Tomlinson	2003	The Differentiated Classroom
9. The Role of the School Leader	Michael Fullan	2007	The School Leader's Guide
10. The Importance of Professional Development	Michael Fullan	2007	The School Leader's Guide

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VCCSA Sequence

System Agent core

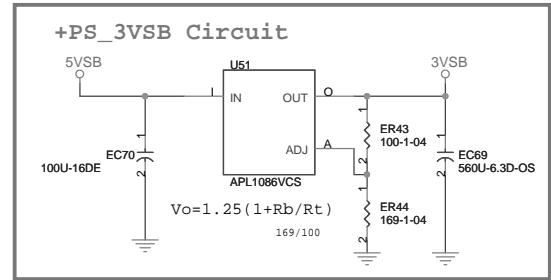
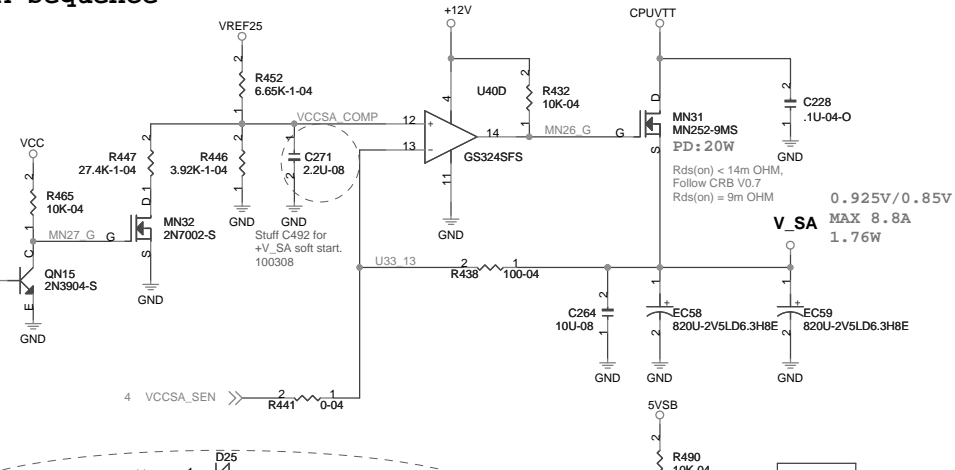
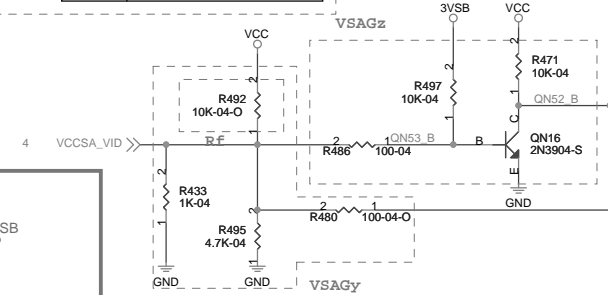
Default Stuffed:

Stuff VSAGz

VCCSA voltage selection	
VID	V_SA
0	0.925V
1	0.85V

Stuff VSAGz

VCCSA voltage selection	
Rf	V_SA
unstuff	0.85V
stuff	0.925V

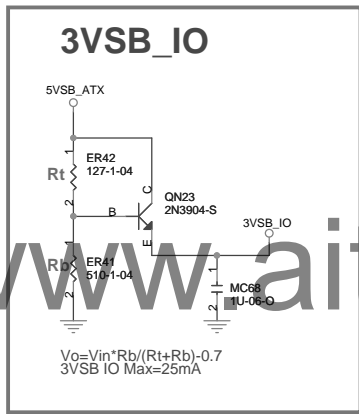


3VSB Non-EuP Lot6 Mode:

Power Name	Current
4 Slots	0.375 X4 = 1.5A
LAN	16m + 49m = 65mA
PCH	123mA
EPW	16mA
SPI	mA
SIO	mA
Total Current	+ 1.754 A

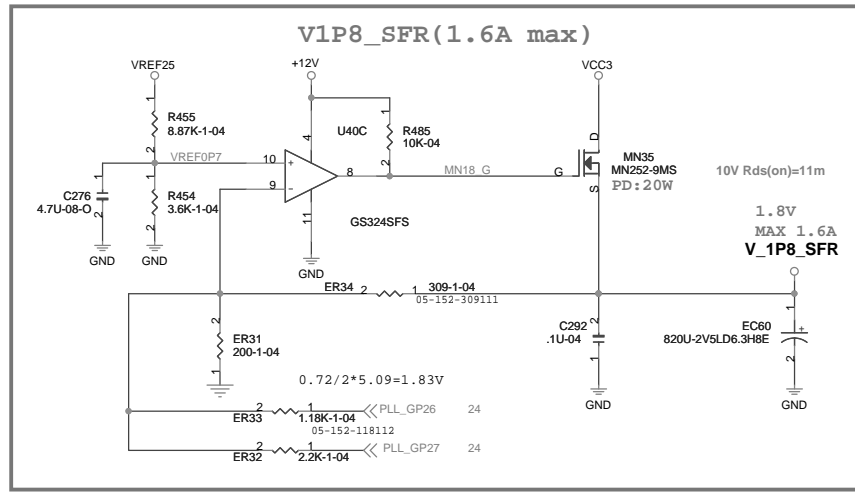
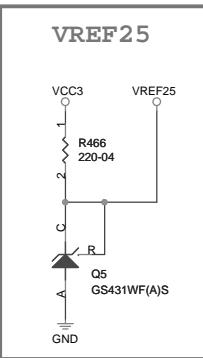
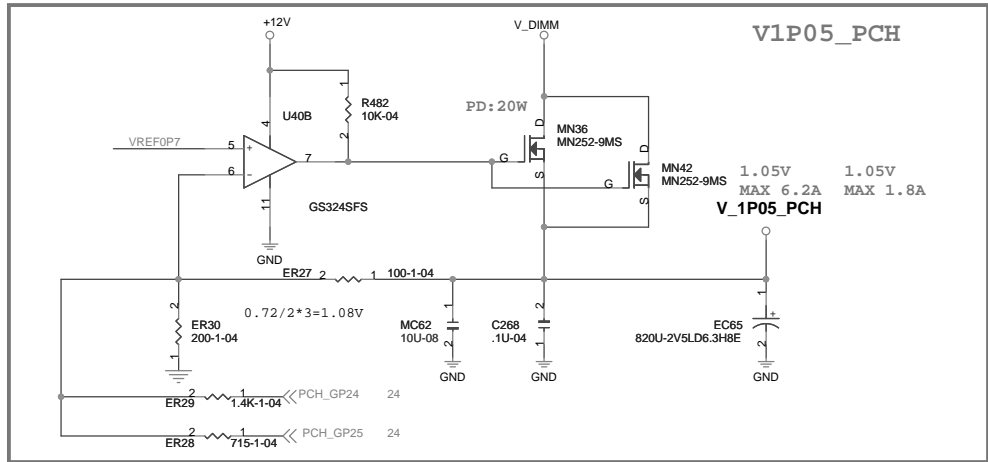
H/W Monitor :1.05V (Traget)

GP26	GP27	PLL
1	1	1.83V
1	0	1.93V
0	1	2.02V
0	0	2.13V



H/W Monitor :1.05V (Traget)

GP24	GP25	PCH
1	1	1.08V
0	1	1.13V
1	0	1.18V
0	0	1.23V

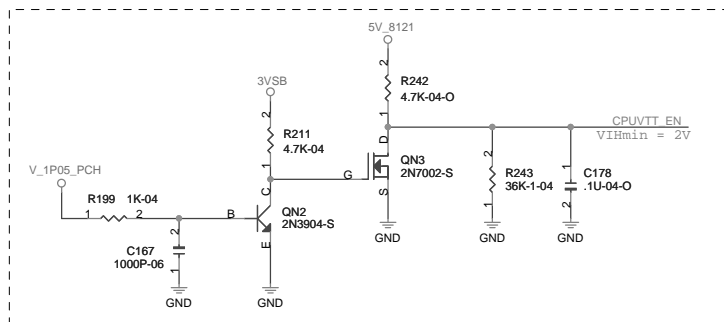
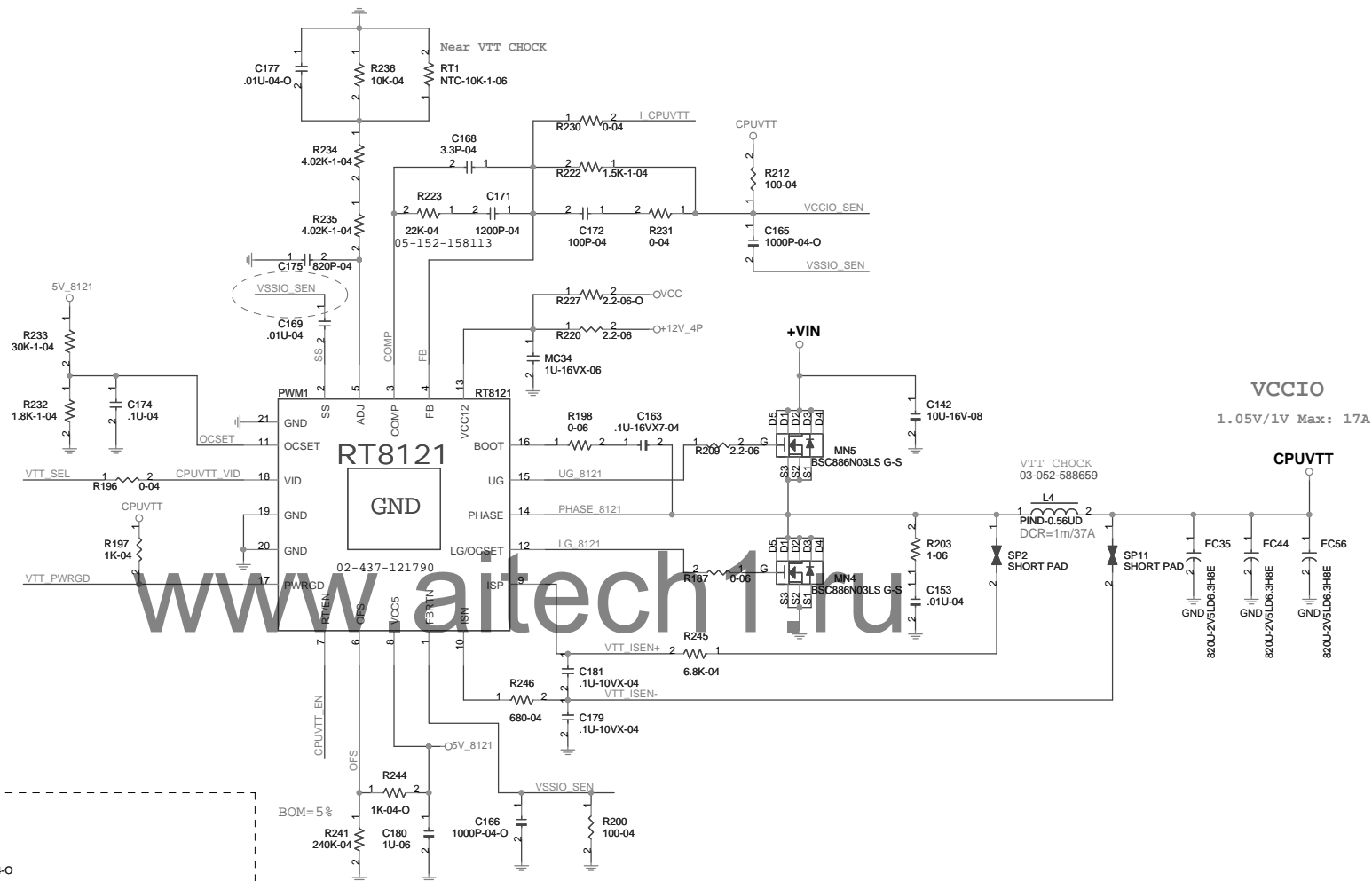


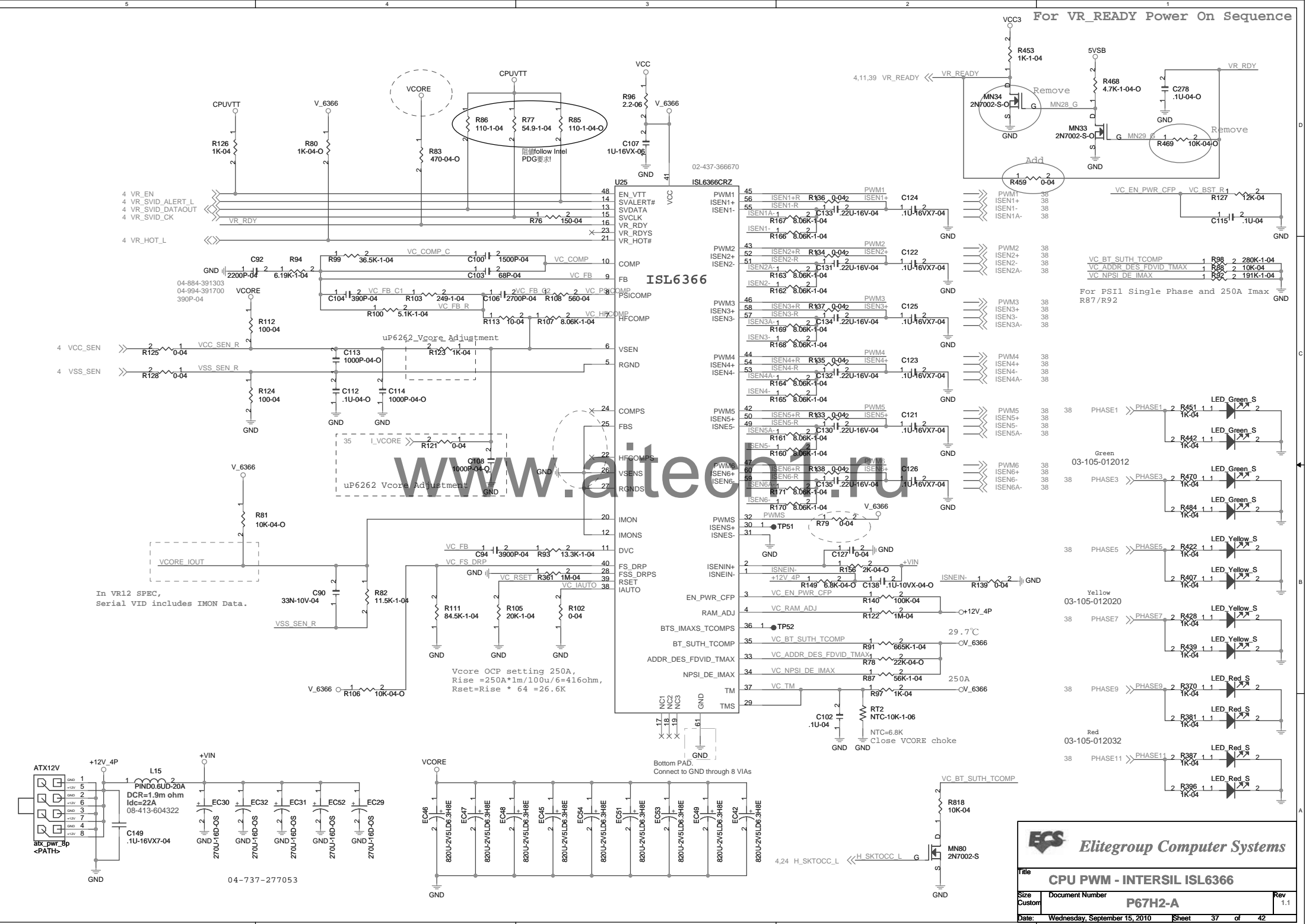
External Connection

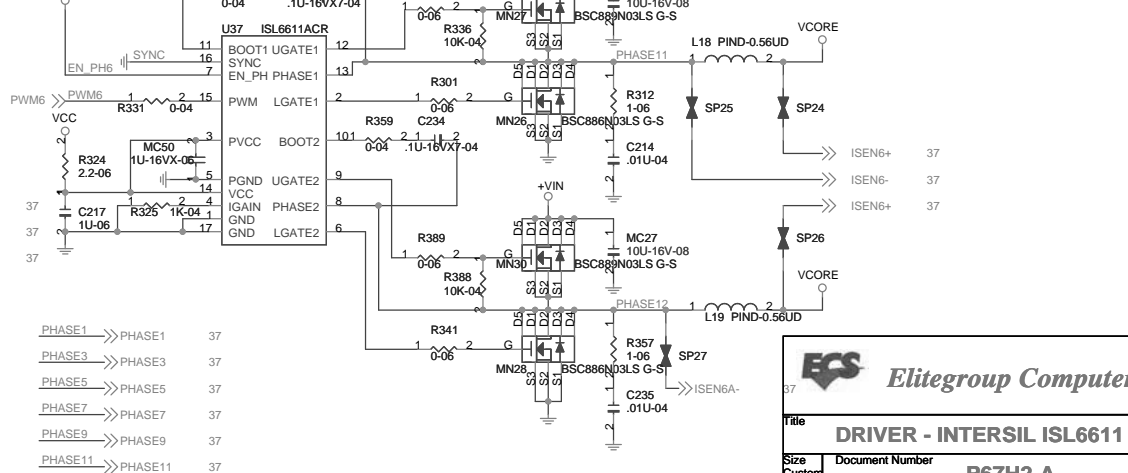
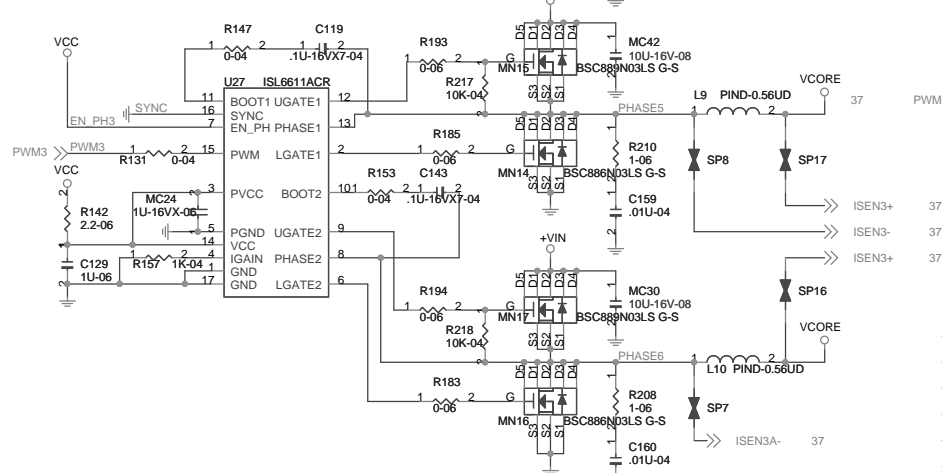
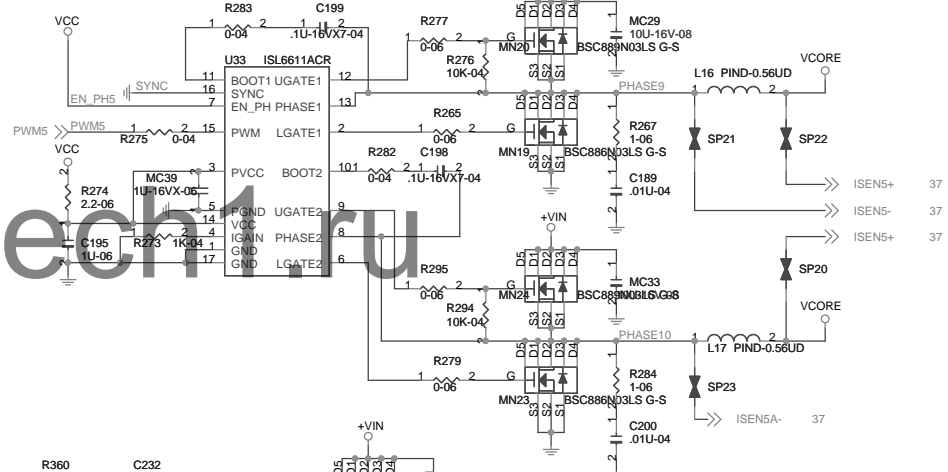
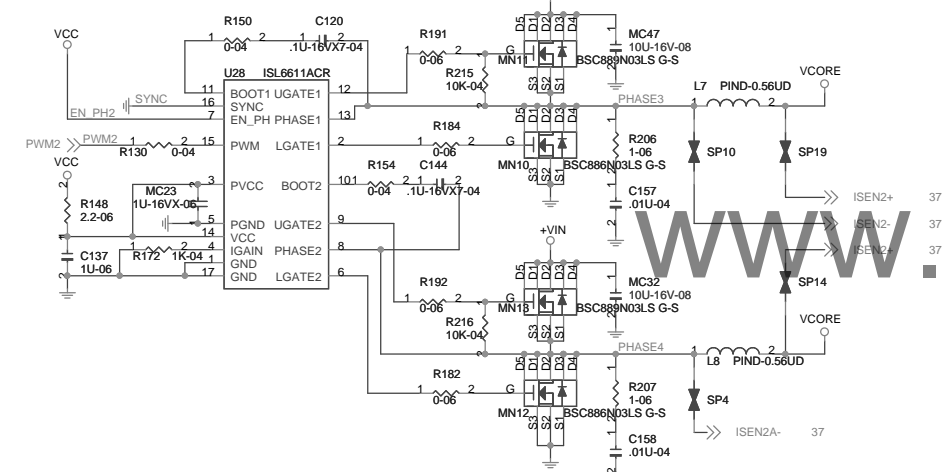
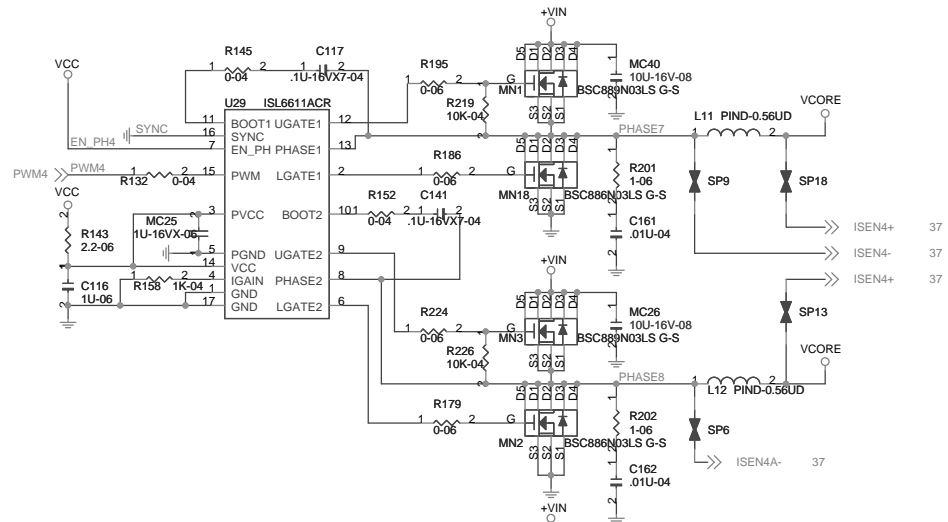
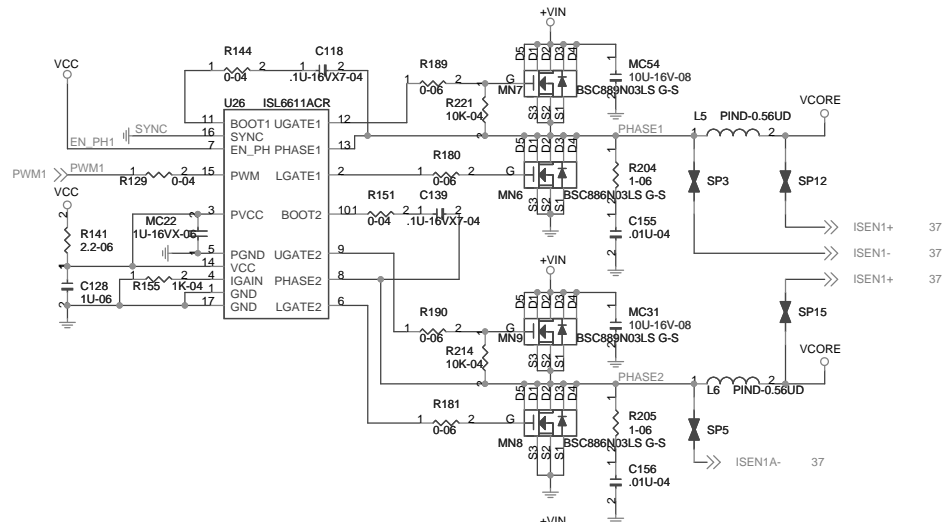
The diagram illustrates the external connections for the microcontroller. It shows a 40-pin package with the following connections:

- VCC to Pin 1
- +12V_4P to Pin 2
- 3VSB to Pin 3
- 5VSB to Pin 4
- V_1P05_PCH to Pin 5
- CPUVTT to Pin 6
- VTT_SEL to Pin 4
- VTT_PWRGD to Pin 34
- VCCIO_SEN to Pin 34
- VSSIO_SEN to Pin 4
- I_CPUVTT to Pin 35

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V







PHASE1 >>> PHASE1 37

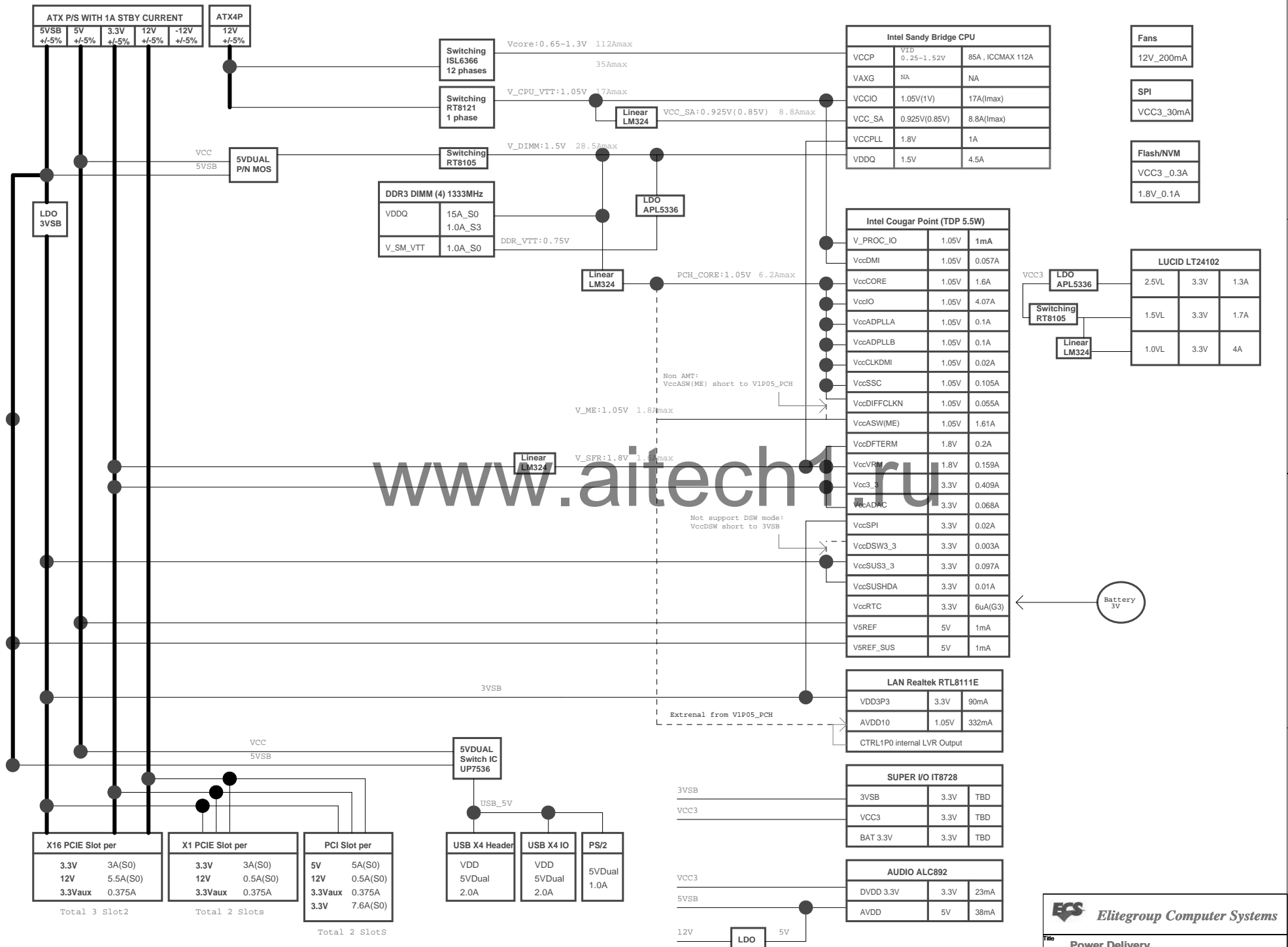
PHASE3 >>> PHASE3 37

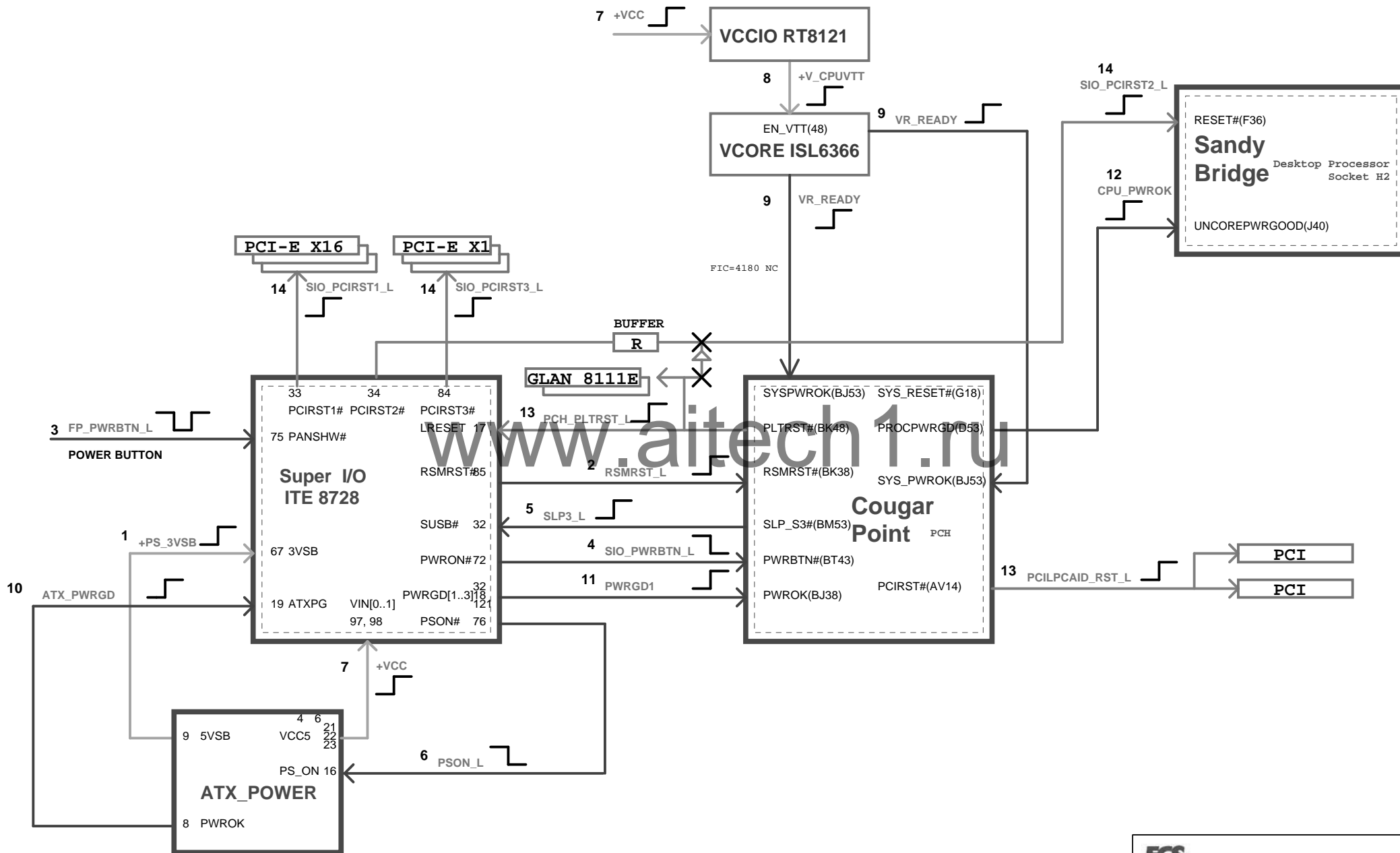
PHASE5 >>> PHASE5 37

PHASE7 >>> PHASE7 37

PHASE9 >>> PHASE9 37

PHASE11 >>> PHASE11 37





NOTE:

Sugar Bay Platform has two clock mode:

- 1.Integrated Clock Mode (Generate by PCH)
- 2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

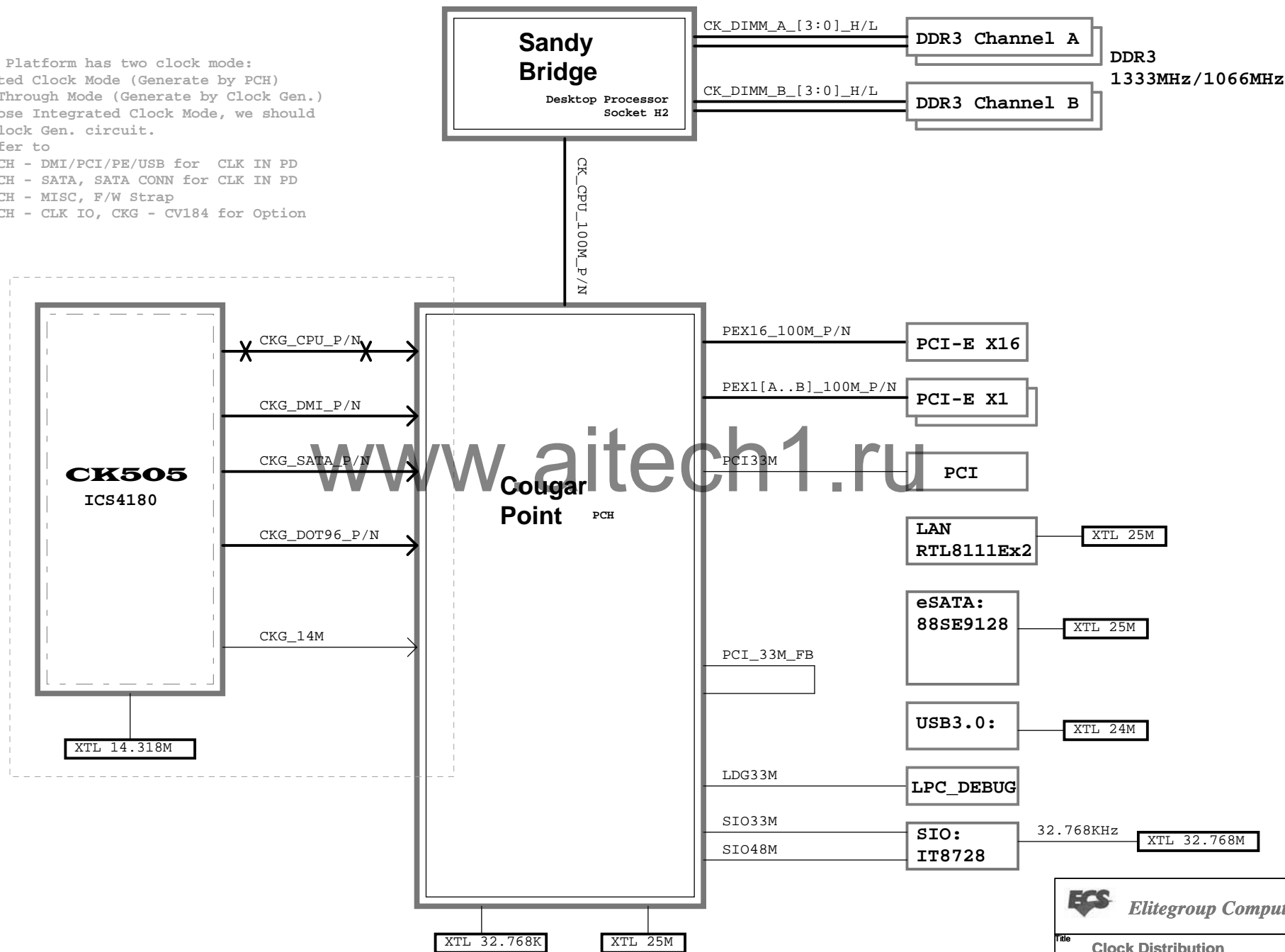
Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option



Elitegroup Computer Systems

Title			
Clock Distribution			
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Custom	P67H2-A	1.1	
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